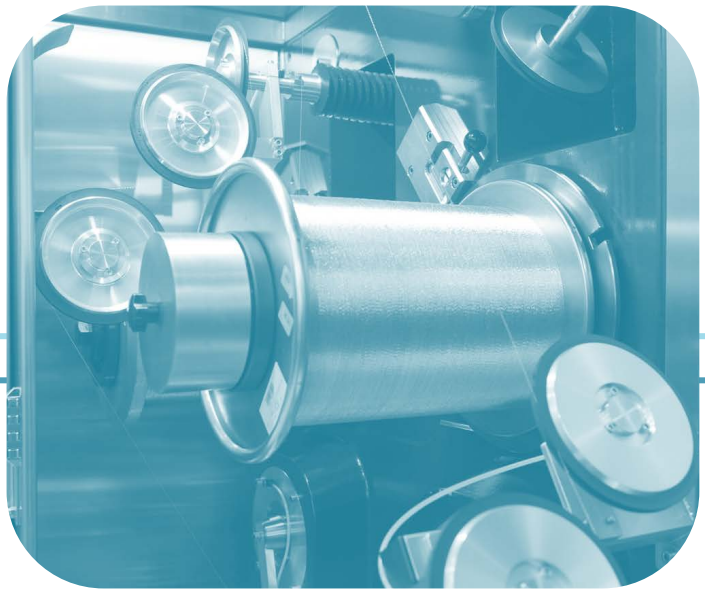
ADVANCED WIRE SAWING TECHNOLOGY
FOR SOLAR PHOTOVOLTAIC CELLS



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INTRODUCTION

For solar cells to be competitive in an energy supply market ultimately driven by the cost per watt, the Total Cost of Ownership (TCOO) of each production step in the PV value chain (Figure 1) takes on critical importance. The manufacture of crystalline silicon wafers is no exception: the TCOO for a processed wafer is a key driver of overall cost.

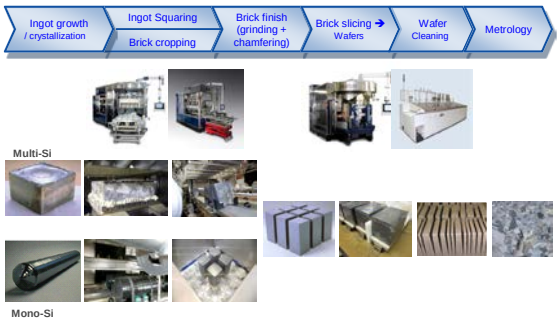

Figure 1: c-Si PV wafering value chain

Figure 2: The Applied HCT Squarer

The wafering process begins with solid ingots made of single-crystal or multi-crystalline silicon material. Wire saws shape the ingots into squared blocks (Figure 2), then slice them into thin wafers. These wafers are used as the base for the active PV cell. Wire sawing is nowadays largely – if not exclusively - achieved by means of Multi-Wire Saw technology (MWS).

This document offers an overview of the wire sawing process and its manufacturing challenges, showing how next generation wire sawing technology can lower the cost of both squaring and wafering.

WIRE SAW HISTORY

The first practical machine for PV wafering was introduced in the mid 1980s, based on the pioneering work of Dr. Charles Hauser, founder of HCT Shaping Systems, Switzerland. (Now the Precision Wafering Systems division of Applied Materials.) These machines used a moving wire carrying abrasive slurry to create the cutting action. Even now, the most prevalent type of saw for shaping and slicing wafers from ingots retains the same basic architecture as Dr. Hauser's original machine, but with greatly increased load capacity and cutting speed.

THE SAWING PROCESS

The heart of a modern wire saw is a single steel wire, 110µm-140µm in diameter, wound on wire-guiding rollers. This wire guide is carefully grooved at a constant pitch, forming a horizontal net, or web, of parallel wires (Figure 3). Powerful drives move the entire web at the same relatively high speed (10-20 m/s). The slurry, a suspension of abrasive particles in coolant fluid, is fed onto the moving wires by manifolds (or "nozzles"). The wires transport the slurry into the cutting zone. The silicon material to be

cut is fixed to a table that moves vertically against the cutting head. This motion pushes the material through the wire web, producing a large number of bricks or wafers simultaneously. In a slurry-based MWS, the cutting action is essentially that of a fast three-body lapping process characterized by a rolling & indenting cutting mechanism [1].

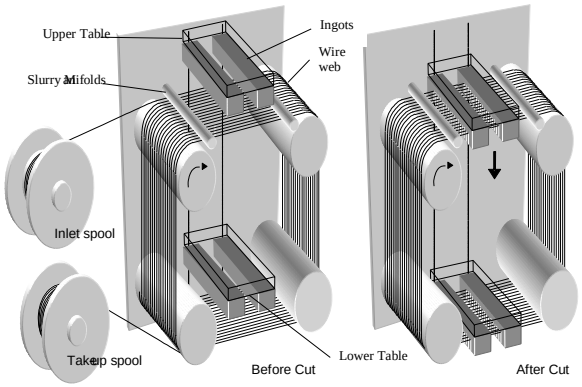

Figure 3: Schematic of a multi-wire saw. Silicon blocks are passed through the web of cutting wires.

The sawing principle is straightforward; the challenge is in the execution. The wire saw must precisely balance the wire diameter, cutting speed, and total cutting surface area in order to achieve precise geometry control and high yield without wire breakage.

REDUCING COSTS

The TCOO of a MWS in wafering applications depends on 4 key elements, in decreasing order of importance: polysilicon market price, wafer yield, cost of slicing consumables, and productivity.

Yield improvement offers the greatest leverage in reducing wafering costs, while little or no action is possible on raw material cost. The wafer yield, defined as the usable surface of wafers produced per unit mass of raw material, is affected by two detractors: the loss of raw material due to the slicing process ("saw dust" or kerf loss) and the cost of any out-of-specs wafers produced by the cut. Silicon usage can be improved by reducing the kerf loss, or by reducing the thickness of the wafers while maintaining the cutting quality. The wafer thickness is defined by the pitch of the wire guide, while the kerf loss depends on the wire diameter and the abrasive grit size. Over the past decade, silicon PV wafer thickness has been reduced from 330µm to today's typical 180 µm thickness, and this trend is expected to continue. The wire diameter, meanwhile, has been reduced from 180-160µm to today's typical range of 130-100µm.

Crystalline silicon PV cell manufacturers demand extremely high wafer quality, with no or minimal surface damage (micro-cracks, saw marks), minimum topography defects (warp, bow and thickness variation) and minimal need for additional downstream processing. As discussed below, wire diameter and grit size are important factors in wafer surface quality.

Finally, consumables cost and productivity enhancement offer additional avenues for cost reduction. Slurry consumption, wire wear, slurry recycling, and wire replacement time can all play a role. Recycling in particular has become a very powerful and efficient tool for cost reduction in a wafering plant. From their market introduction in the early 2000s until today, recycling technologies based on mechanical and chemical separation principles have consistently and markedly reduced slurry cost while providing

environmental benefits. Today, most end-users are slicing wafers with a mix of slurry composed of 70% to 80% recycled components (i.e., liquid coolant and abrasive SiC grit) complemented by virgin materials.

MAIN PROCESS VARIABLES

The goal of the wafering process is to increase throughput while maintaining best in class yield. Throughput is defined as the number of wafers produced in a given time, and depends on the following factors:

1) **Table speed** (or feed rate) is the speed at which the cutting table holding the ingot to be sliced passes through the moving wire web. As the ingot enters the web at the start of the cut, pressure builds up between the wires and the silicon. The abrasive slurry sandwiched between them begins to chip at the silicon through an abrasion mechanism refered to as “rolling and indenting”. The delay between the pressure build up and the beginning of material removal causes a bowing of the wire web. Once the material removal rate matches the table’s rate of descent, the cut has reached kinematic equilibrium. For a given table speed and load, this equilibrium is largely determined by the wire speed, the slurry cutting ability, and the wire tension.

2) **Load** – the total cutting area for each run, i.e. wafer area times number of blocks per load then times number of wafers per block. The number of wafers per block is determined by the length of the silicon brick/ingot divided by the groove pitch of the wire guide.

3) **Wire diameter** – a thinner wire diameter means reduced kerf loss. However, thinner wire is more prone to breakage, and the wire wears during the process of cutting. Its change in diameter drives both the risk of wire breakage and the wafer quality. Optimization of wire consumption involves finding the best trade off between wire wear and breakage risk: a system that tolerates more wire wear will consume less wire, but risks more frequent breakage. For a given application (load, wafer thickness, etc.), the higher the ratio of the table speed (or feed rate) to the wire speed (v_T/v_w), the faster the wire wears.

4) **Serviceability** or change-over time – the faster the saw can be serviced between cutting runs, including replacing the wire and slurry, the higher the overall productivity.

Ideally, manufacturers would like to maximize the load size. Cutting a larger volume of silicon at once produces more wafers in a given amount of time, maximizing productivity. The Applied HCT B5 (Figure 4) is the only system in the market that is equipped to handle a larger load size (2 meters) giving manufacturers the flexibility to optimize load in order to maximize productivity without sacrificing yield.

Figure 4: The Applied HCT B5 Wire Saw

Figure 5, 6, and 7 provide metrology charts for 0.85 meter and 1.73 meter loads, demonstrating that load increase can boost productivity without compromising wafer yield. With a 1.73 m load and 210 µm/min table speed, 98% of wafers met specifications set at 30 µm TTV, 20 µm TV, and 20 µm saw mark.

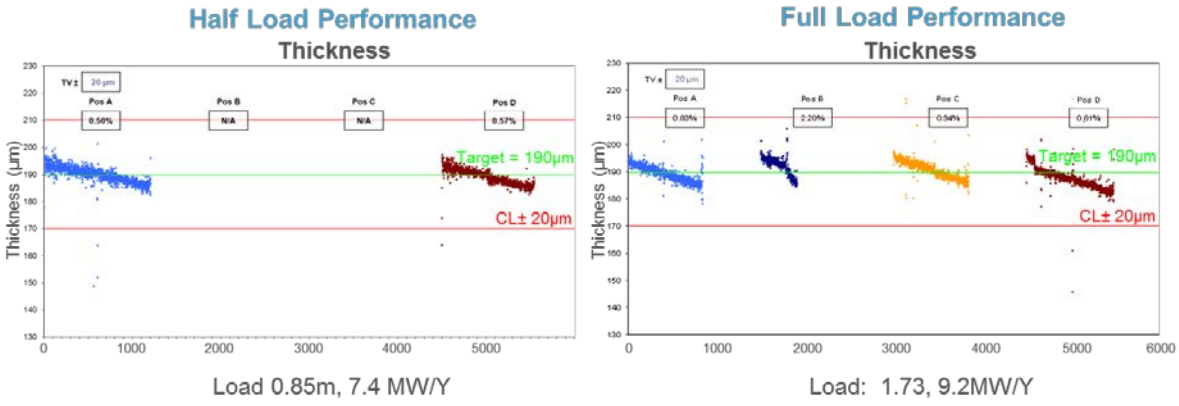

Figure 5: TV Comparison Chart

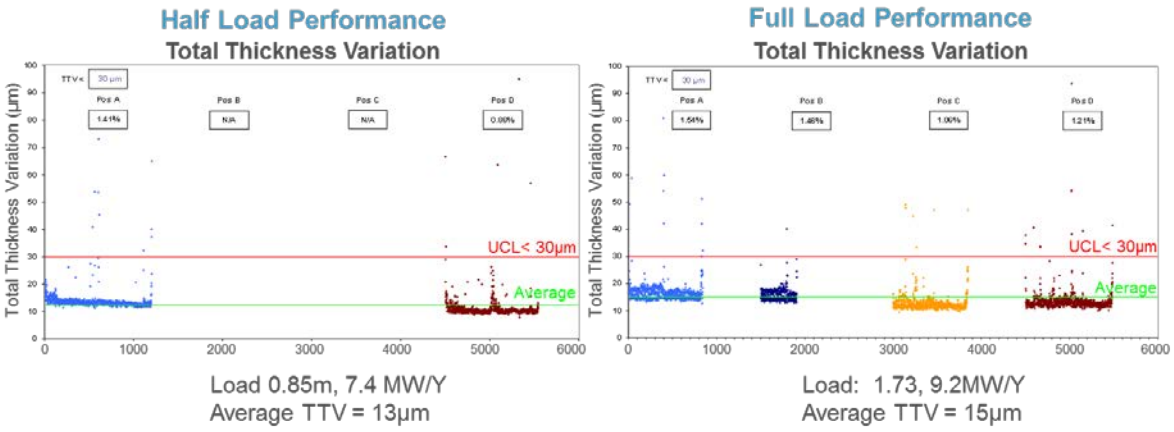

Figure 6: TTV Comparsion Chart

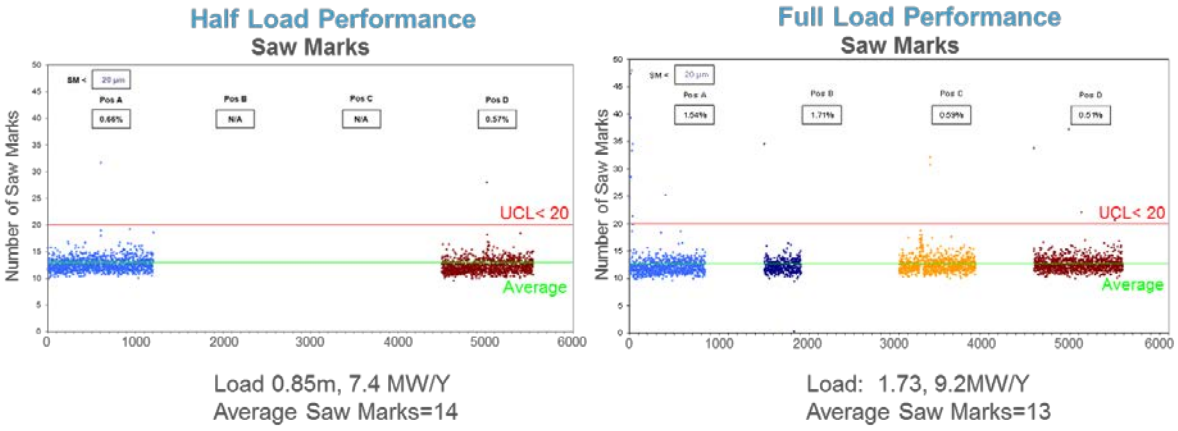

Figure 7 : Saw Mark Comparison Chart

ADVANCED WIRE TECHNOLOGY

To meet market demand for lower costs, wire saw platform architectures must not only allow for load optimization, but must also be able to accomodate advances in wire technology. The B5, a proven wafering system in high volume manufacturing, is capable of handling thin wire and is easily upgradeable to advanced technologies like structured wire and diamond wires.

Figure 8 : Structured Wire

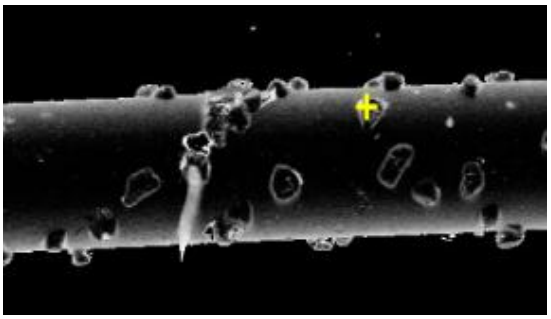

Figure 10: Diamond Wire

Structured wire (Figure 8) is an evolutionary wire technology that can significantly increase productivity due to more efficient transport of slurry and faster cut rate. Applied HCT has pioneered structured wire technology for both wafering and squaring. Proprietary thick structured wire is already proven to increase productivity by 70% and reduce COO by 25% on the Applied HCT Squarer (Figure 9). Applied HCT is currently working on process development for the use of structured wire in wafering applications. The major challenge is the web management of structured wire due to the reduced breakage load. However, we expect to ultimately achieve a faster cut rate with no impact on wafer quality.

BKM comparison	Standard Structured Wire 250µm	Thick Structured Wire 300µm
Kerf loss per ingot (GEN 5 x 250 mm)	2.05 kg per block	2.34 kg per block
Productivity	100%	170%
CoO	100%	75%
Bricks specifications	±0.25mm @ 95%	±0.25mm @ 95%

Figure 9: Structured Wire on Multi Squaring

Next generation diamond wire (Figure 10) is designed to further reduce costs by eliminating slurry while further increasing the cut speed. Diamond wire represents a radical change to the wire sawing process. The diamond wire is essentially a wire surface embedded with diamond particles. The diamond grit size and concentration depend on the application, for instance on whether multicrystalline or monocrystalline silicon material is being sawed. The diamond particles act as the abrasive, eliminating the need for SiC abrasive and resulting in a much cleaner and more environmentally friendly process. As with structured wire, the diamond wire technology is suitable for both wafer slicing and brick squaring applications.

The Applied HCT squarer and B5 platforms can be extended to diamond wire with a hardware upgrade, making the switch to diamond wire technology more cost effective as customers need not invest in a new platform.

Recently, the Applied HCT diamond wire squarer program has achieved a cutting speed of 4,000 µm/min with 100% of bricks in specification in the lab. Meanwhile, Applied HCT is aggressively pursuing a diamond wire wafering solution. Initial results show that monocrystalline silicon cutting with PEG coolant can be easily achieved. The next challenge is to optimize the multicrystalline material load length with water-based coolant in order to completely eliminate PEG recycling cost while still enjoying a high cut rate.

CONCLUSION

As raw material accounts for a large part of the cost of c-Si based solar cells today, wire sawing technology is critical in reducing the cost per watt and allowing PV to reach price parity with grid electricity. Three major advances in wire sawing technology have helped to decrease the amount of silicon material required to produce solar electricity (grams per watt).

First, by enabling the cutting of **thinner wafers**. The historical trend has seen about 50 microns reduction in the wafer thickness every 5 years from 330µm in 1995 to 180µm today. The trend is unlikely to continue at that pace: the increasing fragility of the wafers as the thickness decreases requires advanced automation technology to handle the thin wafers with minimum stress. This is particularly true in the post-slicing step of separating the wafers from the as-sliced stack (also called “singulation”) and in the cell process manufacturing line. Parallel improvements in the slicing process are also needed to reduce thickness variation of the wafer in the same proportion to the thickness.

Second, the use of **smaller abrasive grit** size. The grit size plays a critical role not only in raw material savings by reducing the kerf loss, but also in reducing the “wedge” effect produced by the uni-directional movement of the wire: the wafer is thicker where the wire enters the brick compared to the thickness where it exits. (This variation is ambiguously called “Total Thickness Variation” and is noted TTV.) Smaller abrasive grit also induces shallower surface damage during slicing compared to coarser grits, thereby requiring less saw damage removal in the downstream cell line. Reducing damage also improves the mechanical strength of the wafer, reducing handling losses.

Finally, the reduction of the **wire diameter** over the years has helped save raw silicon material. The wire diameter dropped from 180µm in the mid-1990s to typically 120µm today (with some production excursions at 110µm or even 100µm, and down to 80µm at R&D level).

While the wire saw industry contiunes to reduce the cost of wafering processes based on straight wire technology, emerging wire sawing technologies such as structured wire and diamond wire will further drive down the cost, giving higher productivity and less consumable cost with the same or better wafer quality.

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