OVERVIEW

CADENCE RF SIP METHODOLOGY KIT

The Cadence® RF SiP Methodology Kit accelerates the application of EDA technologies to system-in-package (SiP) designs for Radio Frequency (RF) and wireless applications. It provides methodologies that maximize design productivity and predictability for customers leveraging the advantages of SiP technology. An integrated set of products built around proven methodologies enables complete front-to-back SiP design and implementation. All this is demonstrated on a segment representative design, resulting in reduced time to new products, increased functional densities, and higher system performance.

CADENCE SIP DESIGN TECHNOLOGY

Manufacturers of high-performance consumer electronics are turning to SiP design because it can provide a number of advantages over just SoC. In addition to reduced cost, lower power, and higher performance, SiP design offers the flexibility to mix radio RF and high-speed digital circuitry in the same package. However, this also means it requires expert engineering talent in widely divergent fields. Conventional EDA solutions have failed to automate the design processes required for efficient SiP development. By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on printed circuit boards (PCBs), the Cadence SiP design technology streamlines the integration of multiple high-pin-count chips onto a single substrate. This approach allows companies to adopt what were once expert engineering SiP design capabilities for mainstream product development. Cadence SiP solutions seamlessly integrate into Cadence Encounter® for die abstract codesign, Cadence Virtuoso® for RF module design, and Cadence Allegro® for package/board co-design.

CADENCE RF SIP METHODOLOGY KIT

The Cadence RF SiP Methodology Kit leverages new SiP technologies and verified advanced methodologies for RF SiP design. It enables wireless design teams to achieve predictable design schedules by boosting design productivity while also increasing the likelihood of first-pass success by improving quality. By combining comprehensive links between system design, physical implementation and manufacturing, the kit allows full-SiP electrical analysis and characterization of critical paths as well as behavioral modeling from overall system-level simulation through bottom-up verification.

These capabilities are demonstrated on a segment representative design (an 802.11b/g WLAN RF SiP) that includes a Helic-based RF transceiver and analog baseband die in a 180nm generic CMOS process, a second AMS analog front-end baseband interface die in a 90nm generic CMOS process, and embedded and discrete passive off-chip components in a generic LTCC substrate. The kit also contains re-usable, pre-configured components from test-benches, models, and simulation plans for block and full SiP-level verification and physical implementation approaches. Additionally, design teams are led through a step-by-step example on how to apply advanced Cadence technologies to best achieve design success.

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A design team can use the segment representative design as a basis for understanding the methodology, and then map the demonstrated techniques and technologies to their own designs. This helps the team develop a realizable action plan to improve its own design process. The step-by-step approach further allows a team to absorb and understand a wide array of technologies that can optimize complex RF SiP designs.

KEY BENEFITS

- Combines system design, physical implementation and manufacturing in a complete, true IC/package co-design solution
- Provides a seamless flow starting at full-SiP electrical simulation, through a single schematic-driven layout implementation and ends with comprehensive signal integrity checks
- Achieves functional, performance, and closed-loop verification across multiple technologies and design domains including system-level, digital, mixed-signal, and analog/RF
- Improves simulation accuracy and completeness by effectively combining signal integrity analysis at SiP and parasitic extraction at IC-level
- Optimizes on- and off-chip configurations by managing inductor synthesis and passive component modeling
- Delivered with five days of applicability consulting and expert advice to help jumpstart and fine tune the RF SiP design process

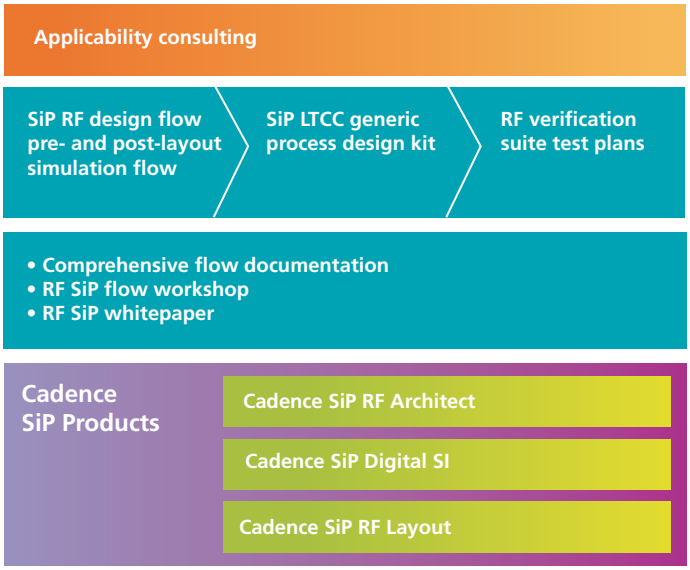

Figure 1: Cadence RF SiP Methodology Kit

KIT COMPOSITION AND INTEGRATION

THE CADENCE RF SIP METHODOLOGY KIT INCLUDES THE FOLLOWING NEW CADENCE SIP TECHNOLOGIES:

- **Cadence SiP RF Architect**

  Cadence SiP RF Architect provides the integration and flow environment linking the Virtuoso® Analog Design Environment (ADE) and Cadence SiP RF Layout. It enables the creation of a single simulation-capable top-level SiP RF Module schematic that includes the RF/analog ICs that are part of the final SiP design. It provides schematic-level prelayout definition and characterization of substrate-level embedded RF passive devices, as well as a bi-directional ECO and LVS flow between the substrate layout and the Virtuoso ADE environment. RF/Analog ICs can be exported from the Virtuoso Layout Editor as design-ready SiP die footprints, including post-wafer-processing geometry adjustments.

- **Cadence SiP RF Layout**

  Cadence SiP RF Layout comprises a physical detailed implementation environment for complete SiP RF substrate place and route. It includes final connectivity optimization, die stack creation, support for flipchip and wirebond attach die, RF embedded passive creation and optimization, manufacturing preparation, full design validation, and tapeout.

- **Cadence SiP Digital SI**

  Cadence SiP Digital SI fully integrates digital signal integrity (SI) analysis, interconnect extraction, and modeling with the physical SiP design environment. By combining proven SI technology in an environment that permits interactive editing of die-to-die and substrate interconnect, SiP design engineers can optimize a design to meet both electrical and physical requirements—while achieving reduced design cycle times.

THE CADENCE RF SIP DESIGN METHODOLOGY KIT RELIES ON AND INTEGRATES WITH THE FOLLOWING VIRTUOSO TECHNOLOGIES (NOT INCLUDED):

- **Virtuoso Schematic Editor**

  As the design composition environment for the Virtuoso custom design platform, Virtuoso Schematic Editor delivers an extensive set of tools for custom IC design entry. From architectural definition using industry-standard language representations, such as Verilog®, VHDL, and C, to final structural implementations at the transistor level, it aids in the implementation of each stage in a design.

- **Virtuoso Analog Design Environment**

  The Virtuoso Analog Design Environment is the analog design and simulation environment for the Virtuoso custom design platform, and the industry's standard task-based environment for simulating and analyzing full-custom, analog, and RF IC designs. It features a graphic user interface, integrated waveform display and analysis, distributed processing, and interfaces to popular third-party simulators.

- **Virtuoso Multi-Mode Simulation**

  Virtuoso Multi-Mode Simulation combines four fast, silicon-accurate simulation engines (Spectre®, AMS Designer, Spectre RF and UltraSim) into a comprehensive solution for analog, mixed-signal, RF, and full-chip design verification. Advances in design methodologies and flows require a mixed approach to simulation. Virtuoso Multi-Mode Simulation delivers the SPICE, FastSPICE, RF, and analog mixed-signal capabilities to simulate any analog, mixed-signal, or RF design.

- **Virtuoso Passive Component Model (feature of Spectre RF Simulation Option)**

  Virtuoso Passive Component Modeler (VPCM) is an inductor synthesis, modeling, and verification tool. It comes tightly integrated into Cadence Virtuoso custom design platform. RF designers can use VPCM as a vehicle to synthesize/verify an inductor, while RF modeling engineers can also use it to generate inductor models based on measurement data or EM solver output data and automatically generate a PDK, including parameterized layout PCell view, schematic view, symbol view, etc. To help make tradeoffs between speed and accuracy, the VPCM synthesis module includes three different synthesis algorithms: quasi-static EM solution, full-wave EM solution, and scalable equivalent circuits.

- **Virtuoso XL Layout Editor**

  Virtuoso XL Layout Editor is the high-end custom block authoring physical layout tool in the Virtuoso platform. It supports the physical implementation of custom digital, mixed-signal, and analog designs at the device, cell, and block levels.

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

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