EMC Design Guidelines For Electronic Modules

The objective of this document is to incorporate EMC “lessons learned” from previous designs into new designs so that EMC compliance can be achieved earlier in the design cycle.

This document is intended for person(s) responsible for the design/layout of electronic modules.

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1.0 Change Control

Document Request Change Date	Page # changed	Reason for Change	Date Issued	Revision Number
		Initial document release	3/1/99	00

If there are any questions concerning this document
Please contact one of the following individuals.

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2.0 Beginning Comments:

- If all recommendations are followed within this document your chances of meeting component and vehicle level EMC requirements will have increased significantly.

- If recommended components are thought to not be necessary, it is recommended that “place holders” or provisions for all of the components be placed on the circuit board. It is easier and cheaper to remove the provisions later (if not necessary based on testing) then to have to ADD them later.

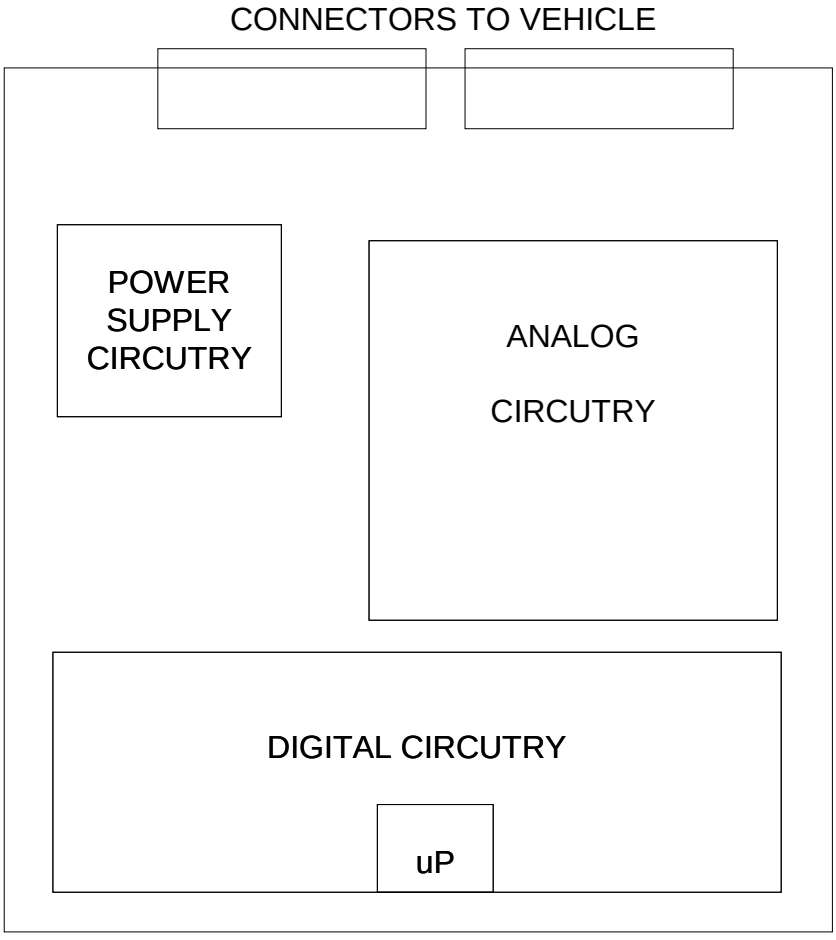
- Always provide test data to support claims that any of these recommendations will have negative results on product performance.

- Do not use socketed IC’s when making measurements. Especially when measuring for ringing.

- If there is any change within your module, it is necessary to retest radiated emissions and radiated immunity at a minimum. “A change” is defined as:
    - Microprocessors type, package size, manufacturers
    - Memory size or type
    - Board layout changes, trace placement, parts add
    - Connector change, location, type

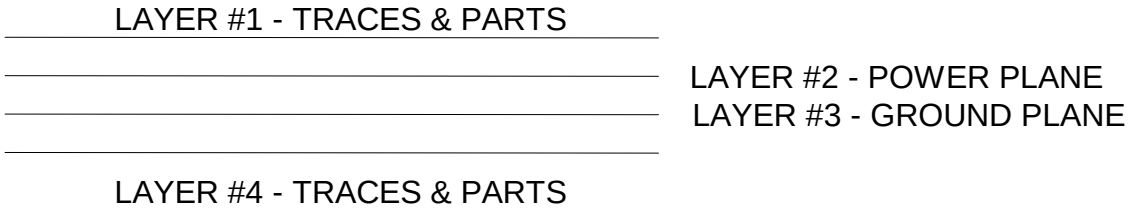
3.0 Zones

- Group all analog circuitry together to create an analog zone and group all digital circuitry together to create a digital zone.
- Locate the power supply zone close to the vehicle harness connector.
- Locate the Analog I/O control circuitry close to the vehicle harness connector.
- Locate all digital circuitry, including all uP's and peripheral hardware, at the back edge of the circuit board on the opposite side of the vehicle harness connector.
- Never place connectors on opposite sides of the board, place them all on the same edge.
- Do not run analog and digital traces parallel to each other.

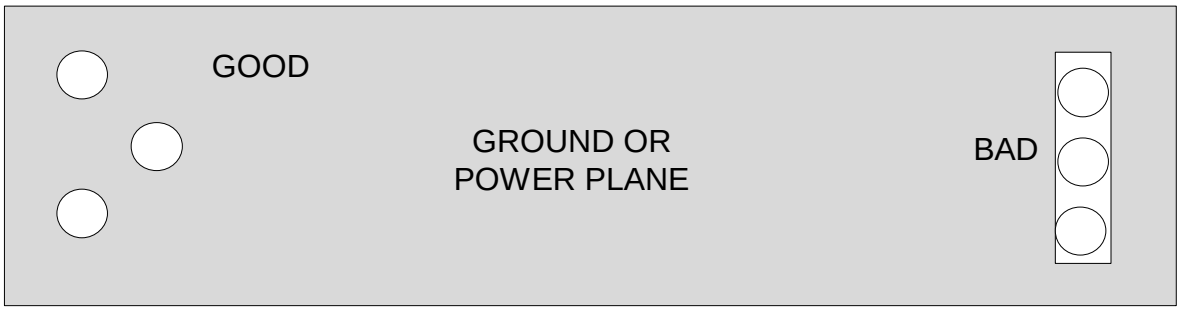


4.0 Planes / Layers

- DO NOT SEPARATE THE GROUND PLANE INTO “DIGITAL vs. ANALOG” or “CLEAN vs. DIRTY” or “5V RETURN vs. 3.3V RETURN vs. 12V RETURN”.
- Multilayer boards are always recommended.
- Route all traces on the outer layers (1 and 4) over continuous power and ground planes, typically layers 2 and 3.



- Be sure to fill all spaces between pass through’s (connector pins and other hole producing items) with plane material. If necessary, stagger the pins of connectors or devices to make room for filling in the area between the legs with plane material.



- Keep both planes uncut, do not route traces on the power and ground planes. If this is necessary, then jump over the trace with 0.1uF or 0.001 uF capacitors (many capacitors if the cut is long). Create a short and direct path for the Vcc from the voltage regulator to the microprocessor on the power plane and ensure that the ground return parallels the Vcc (typically underneath) between the regulator and microprocessor.
- All open spaces on outside layers should be filled with ground plane, these ground “islands” need to be tied to the ground plane with multiple via's or many short, thick (low inductance) traces connecting them all together
- All connections to power and ground planes have to be very short runs (PIN TO PLANE) *(low inductance paths are key)*

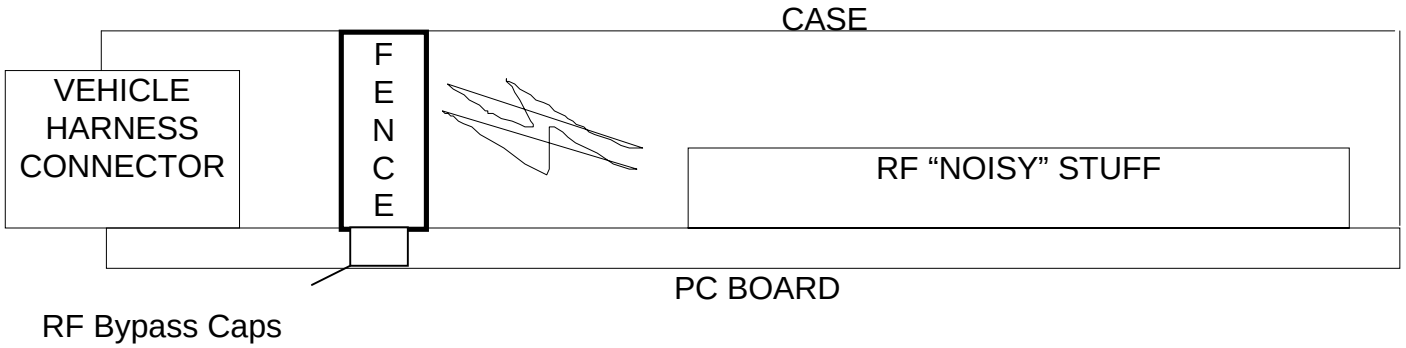
5.0 Shielding

5.1 “Fences”

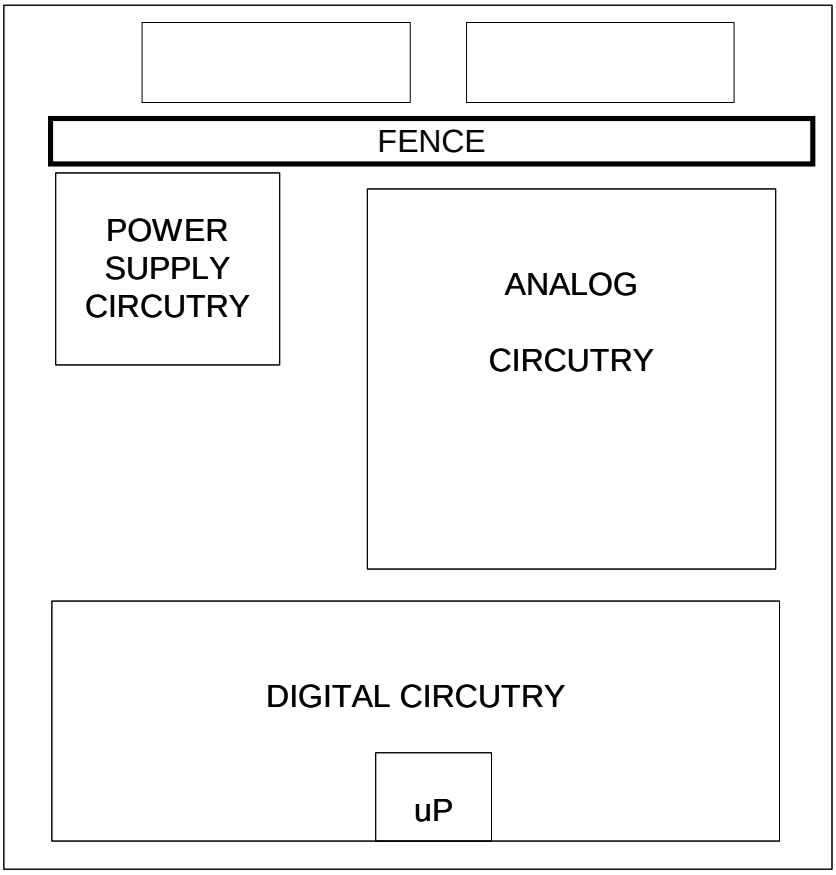
- If possible - use a heat sink type rail, parallel to vehicle harness connector to prevent RF energy from re-coupling onto the vehicle harness connector. This rail is comprised of vertical metallic

wall, created a RF barrier, covering the exposed connector pins. Ground this fence at least every 1/2 inch to the ground plane

- Place RF bypass capacitors which filter the lines to the vehicle harness directly under the fence



- Do not run any traces outside of fence, except those running to the vehicle connector



5.2 Shielded Connectors

- Avoid using shielded connectors (typically costing $5-$7), consider using a folded metallic cover behind the vehicle harness connector tied to the ground plane.
- Filter every pin of the connector with a bypass capacitor to ground. (Even if a shield is not used).

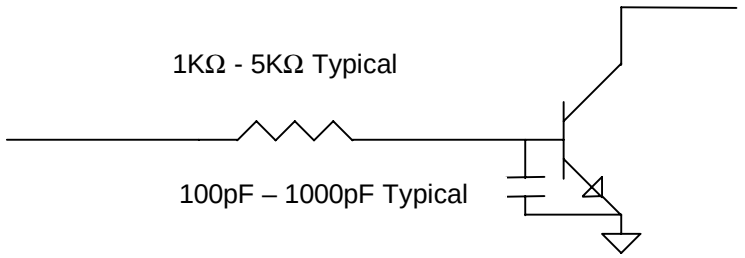
6.0 Traces

- All short unterminated connectors should be removed from the board (i.e. test connectors, diagnostic connectors)
- Avoid sharp 90 degree corners with all traces, instead have gradual bends or two 45 degree bends.
- Any floating or unterminated traces should be removed from the circuit board.
- Try to get as much ground foil as possible under the microprocessor.

7.0 Switched Outputs

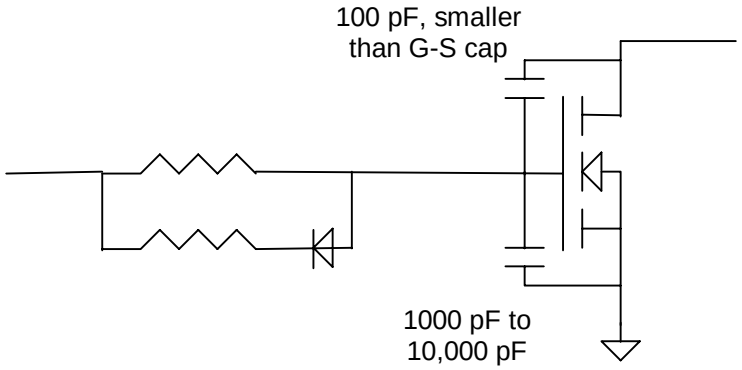
7.1 Low Side Switched Transistors

- Place base resistors (1KΩ to 5KΩ) as close as possible to the transistor.
- SOT23 type transistors (very small package with a very high bandwidth) need a capacitor (100 pF to 1000 pF) between the base and emitter to prevent radiated immunity biasing.



7.2 Low Switched (FETS)

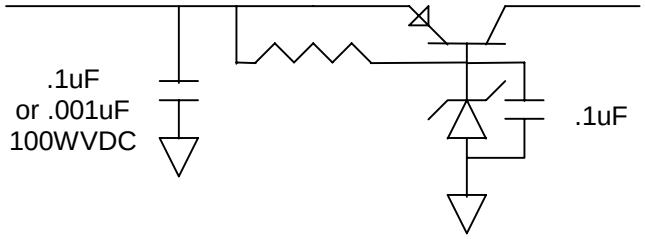
- PWM outputs require a 100 pF capacitor from gate to drain for negative feedback and a capacitor from gate to source (1000 pfd to 10,000 pF) for controlling the switching time. Ideally the rise and fall times should be >1ms/Volt.
- Gate control of rise and fall times with parallel resistor and resistor/diode combination is recommended.



8.0 Power Supplies / Voltage Regulators

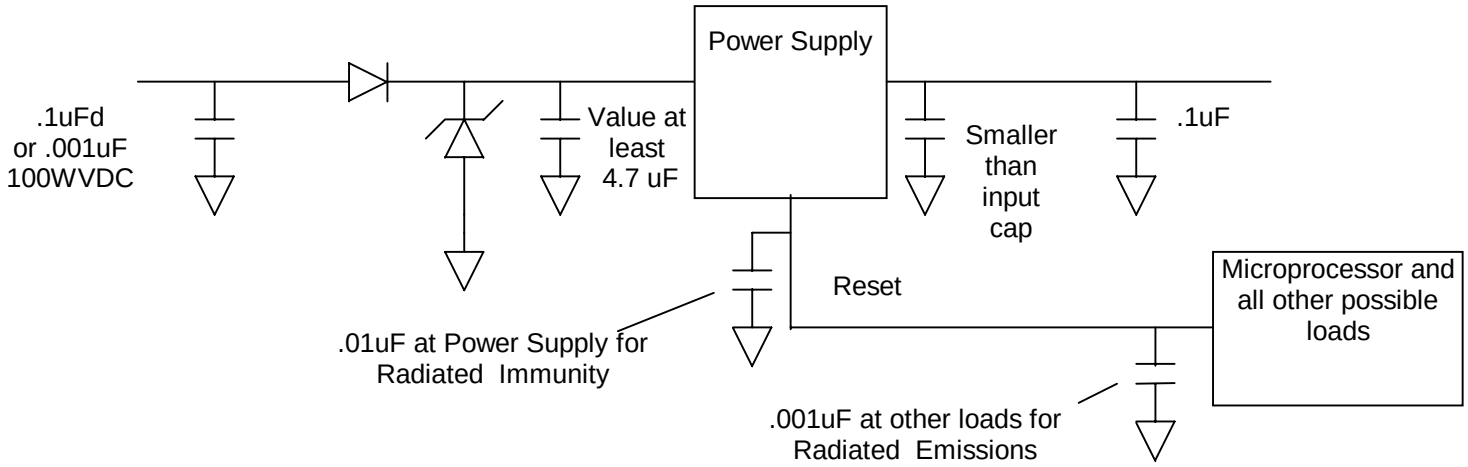
8.1 Zener Supplies

- Place a .01 uF RF bypass capacitor across the zener diode.
- Place a series pass transistor with a base to emitter bypass capacitor ???????
- Place a .1 or .001 uF 100 WVDC (if possible) for ESD protection at the vehicle harness connector.



8.2 Non-Zener Supplies

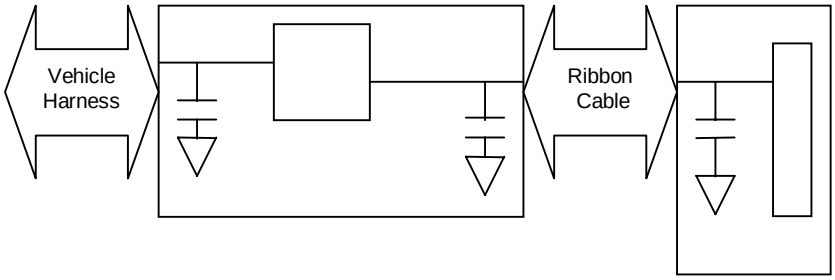
- Place a diode for reverse and one for overvoltage protection at the connector leading to the vehicle.
- Power input should be filtered (20dB at 100 kHz) using bulk storage electrolytic at the entry point, C (uF) = 16/R, R = DC resistive load or 4.7 uF which ever is greater, place a .1 uF SMT low-loss capacitor adjacent to the bulk storage capacitor.
- Reset trace must have RF bypass capacitor (.01) for radiated immunity.
- Reset trace must have capacitor (.001) at all other loads for immunity.
- Input capacitance to power supply must be a larger value than the output capacitance .



9.0 Analog Circuits

9.1 Hardware Filtering

- Place a surface mount (SMT) low-loss, 0.01 or 0.001uF capacitors at each pin of each connector.



- Each analog IC should have .001 SMT low-loss capacitor from VCC to ground physically located at the IC using the shortest trace length possible.
- Switch inputs should have a low pass filter with a time constant of at least 1 ms. Inputs with signals below 20kHz should also have a low pass filter with a time constant set according to the signal.

9.2 Software Filtering

- Analog inputs should have a filter of at least 1 ms (after initial RF bypass cap).
- Use ratiometric comparisons of analog inputs.
- Have realism checks in the software to compare successive reads. If a parameter changed by an amount that is more than it realistically could have in that amount of time, then ignore the read.

9.3 Comparators

- Place provisions for a .001 uF capacitor between each + and – input of each comparitor, placed symmetrically or balanced with little to no trace length.
- Place provisions for 220 pF capacitor from each + and – input of each comparitor to the ground plane with little to no trace length.
- Use resistor dividers not diode drops to set reference voltages.

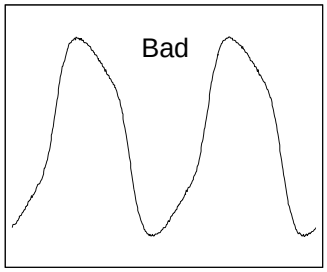
10.0 Digital Circuits

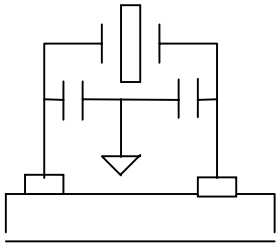
10.1 Digital Traces

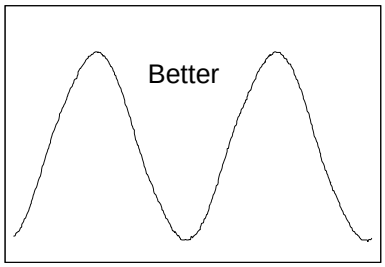
- Cluster all control and address peripherals. Do not stretch them across the board, parallel the traces or daisy chain them.
- Long clock runs should be terminated at the source with a capacitance of 1000 pF.
- Clock cross talk prevention includes separation between digital traces equaling 3X trace width (S/W>3).
- Data cross talk prevention = S/W>1.
- Clock , Reset, and Interrupt traces are sensitive. Do not run them parallel to high-current switching signals. Route them across offending traces or on a “quiet” zone of the board.

10.2 Oscillators

- Phasing capacitors (22-47pF or greater) must be tied directly back to the microprocessor through the lowest inductive path. With a reference trace between the two oscillator traces, add as much capacitance as necessary to condition the waveform to be as smooth or sinusoidal as possible. These caps should be of different values to unbalance the capacitance on the crystal with the larger capacitor on the driven end of the crystal.







10.3 Microprocessors

- Avoid expanded bus as much as possible. This will increase the risk for radiated emissions and immunity problems.
- E-clock traces must be shadowed with ground either side by side or over and under.
- Eliminate ringing on the rising and falling edges of the address, data, and control lines to reduce radiated emissions. This can be accomplished by adding capacitance (50 - 270 pF) at the source.

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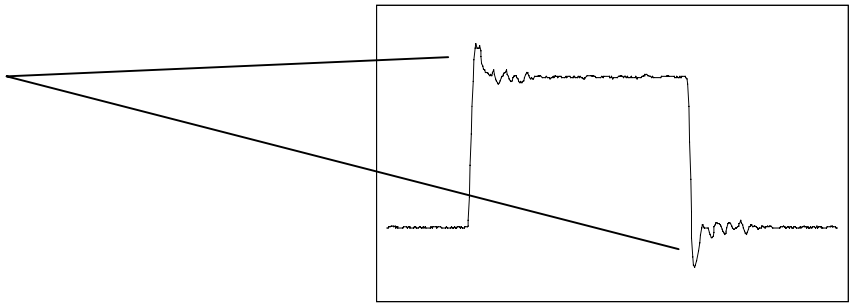
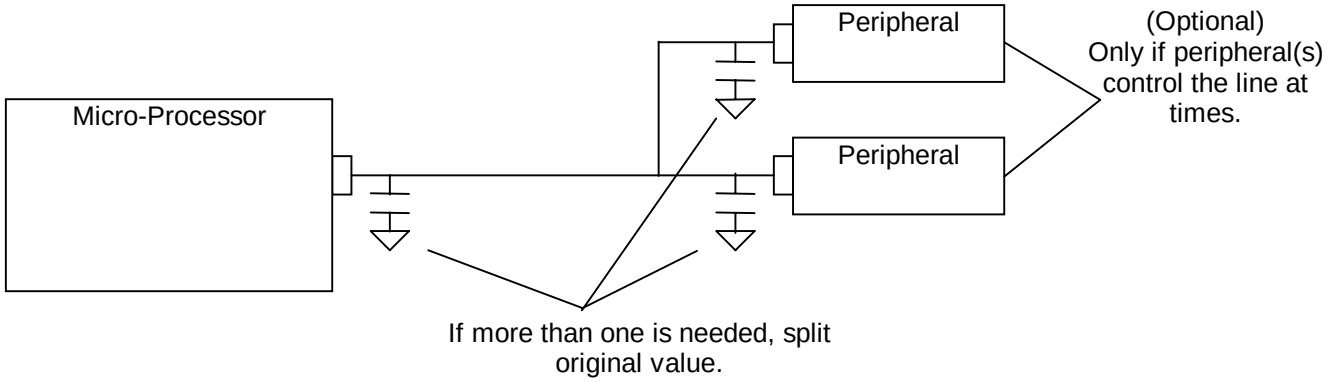
These ringing edges must be eliminated by adding 10-270pF of capacitance at the source(s) to ground
Ideal rise and fall times are > 3nS.



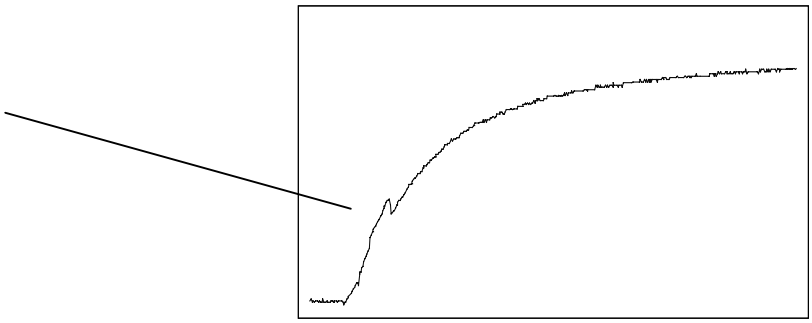
- Slow the rise and fall times as much as possible to minimize the radiated emissions.
- Try to get as much groundfoil under the microprocessor as possible.
- Use the lowest clock frequency that meets the system operational requirements.
- Add capacitance (????value) , next to the microprocessor, from the Reset pin to ground.
- Ground all of the pins of the microprocessor that are not used.

- Data lines should have a capacitor at the microprocessor and a capacitor at each peripheral.

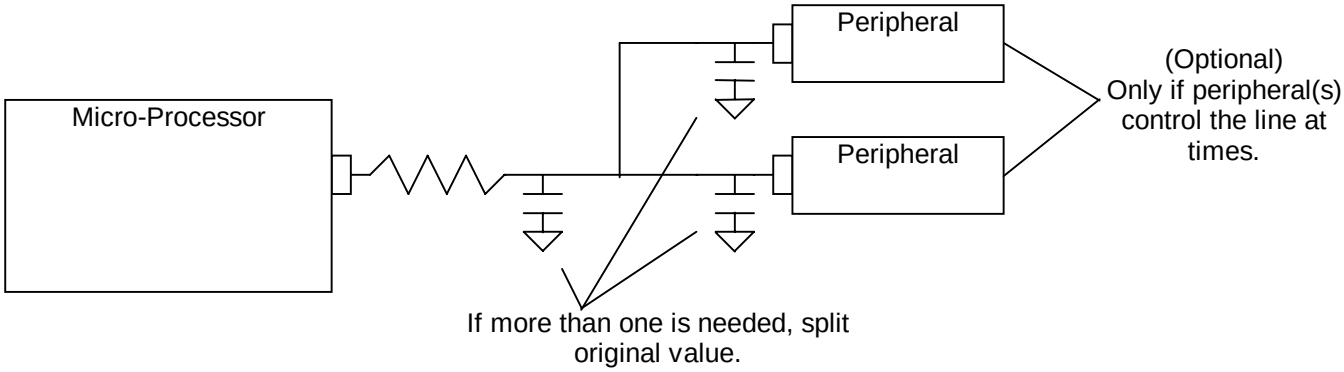


- E-clock and Address lines are to be conditioned with capacitance at the source.
- Non-linear humps on address, data, and control lines must be eliminated to reduce the radiated emissions from the device by adding series resistance <u>at</u> the source(s), typically 50Ω to 250Ω total and a capacitor to ground.

This non-linear "hump" determines that a series resistance (50-250Ω) at the source(s) is necessary to reduce the radiated emissions.
Typically the "hump" is more pronounced.

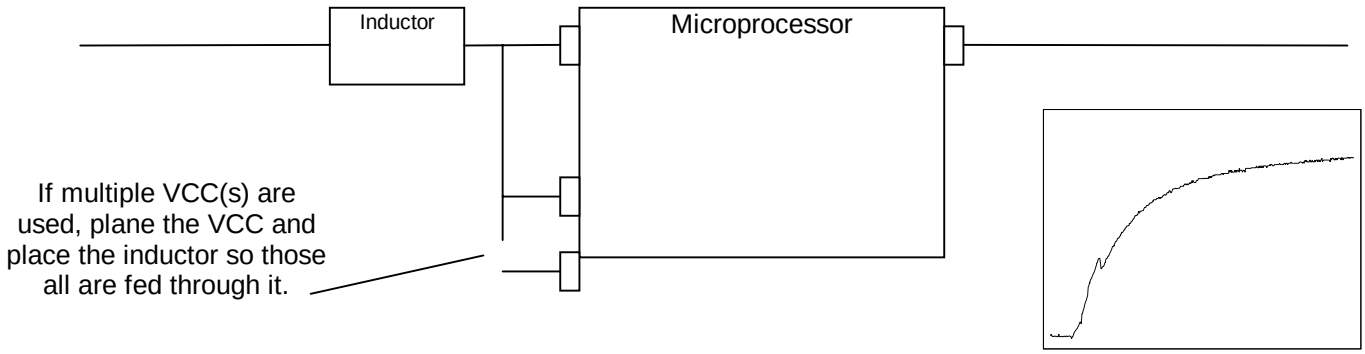


- Values of the resistance will depend on the speed and the current of the devices, it may be best to place 0Ω jumpers at the source(s) to allow changing of the values once the board is created.

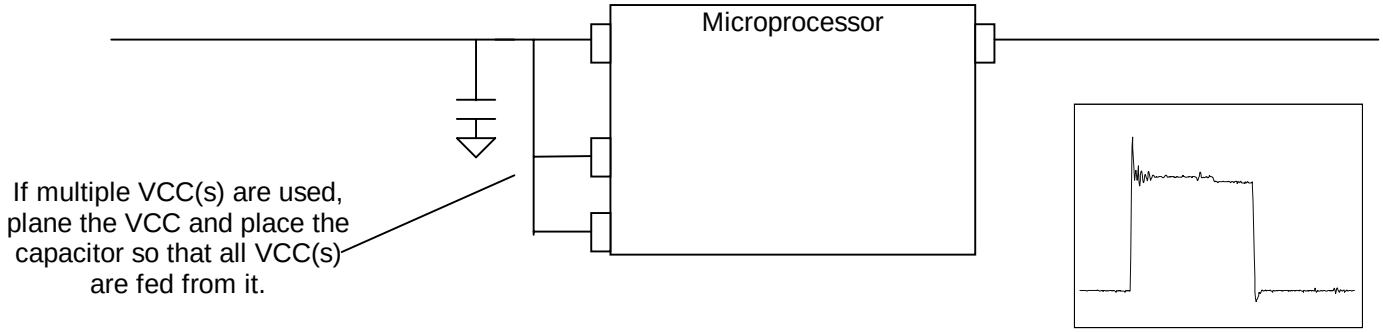


10.4 Microprocessor – VCC Filtering

- It is also necessary to control the VCC currents along with conditioning the address, data, and control lines to reduce radiated emissions from the microprocessor. Filtering one without addressing the other could result in higher radiated emissions.
- A series inductor (BLM32801, 600Ω @ 100 MHz or 1000Ω @ 100 MHz) is recommended for microprocessors which have the "hump" characteristic on its outputs. *(current starving the microprocessor VCC)*



- Capacitance (.1uF to .001uF) is recommended for microprocessors, which do not have the "hump" characteristic on the outputs. Be sure to place the capacitor at the microprocessor and reference it to the ground plane of the microprocessor with a short and fat (low inductance) trace. **REMEMBER PIN TO PLANE, LOW INDUCTANCE CONNECTIONS/TRACES!**

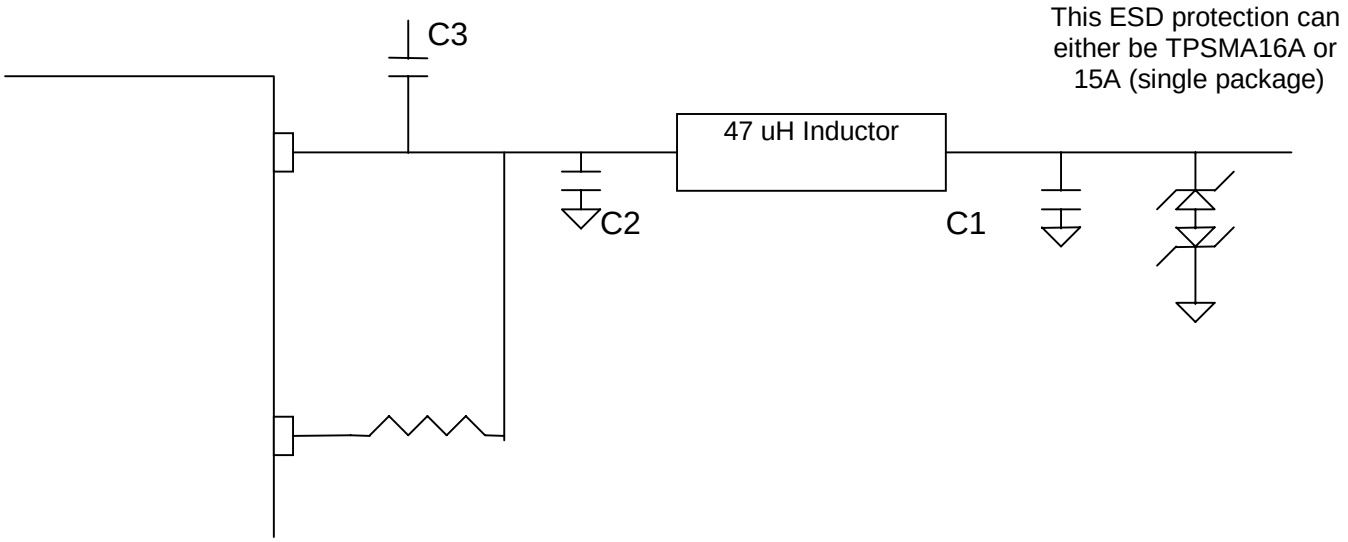


- If the Phase Lock Loop (PLL) portion of the microprocessor has a separate VCC input (Motorola 6808 type) then separate that trace and feed it through a ferrite bead (1000Ω @ 100 MHz) only. In the frequency domain (with a spectrum analyzer) the unconditioned PLL VCC line has harmonics near 80 MHz and 180 MHz.
- For 6805 type microprocessors (w/internal diodes) that have external or internal 12V pull-up, series resistance of 1KΩ is necessary on I/O pulled to 12V.

11.0 Communication Chips

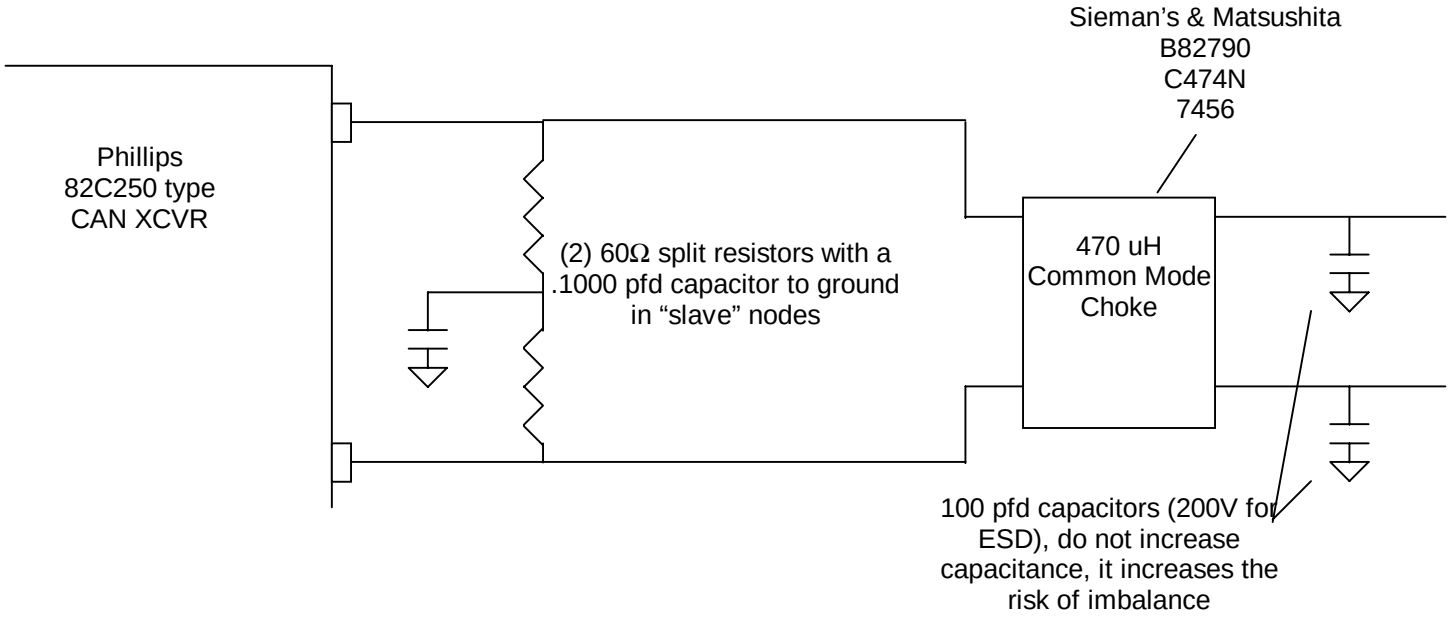
11.1 Class 2 (SAE J1850)

- C1 should be 220 pF and provisions for C2 & C3 are recommended (100 pF each), then a 47 uH inductor, the C2 & C3 provisions may be needed to remedy potential immunity problems found during testing. If C2 is used it will be necessary to change C1 to 100pF.



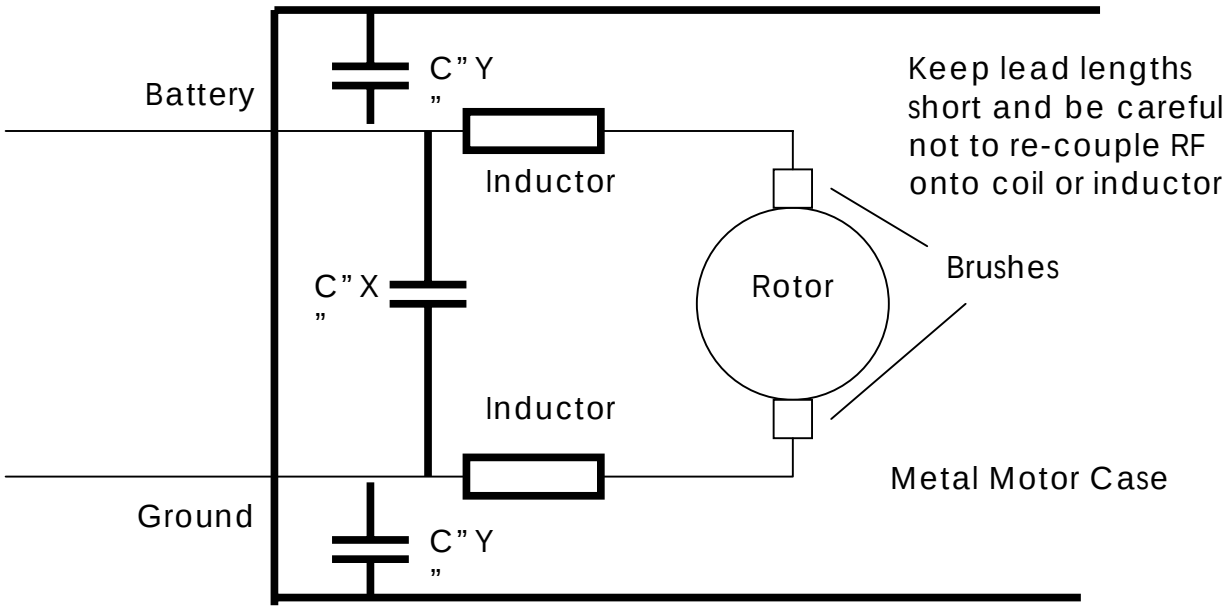
11.2 Dual Wire CAN Buss

- Dual Wire CAN is the lowest risk of all CAN options
- All nodes should be configured as shown below to ensure the best possible EMI performance
- If your node requires a 120Ω termination resistance, refer to figure below for best possible EMI performance



12.0 DC Motors

- The illustration below shows a suppression network for DC motors.



SINGLE DIRECTION:
C" X" =.22uF-.47uF
And tie case to return at brush holder
Inductance Values are
5-10uH for low current
10-20uH for High current. Orient to avoid re-coupling

BI-DIRECTION:
C" X" =.22uF-.47uF
C" Y" (optional) = 0.001uF
Keep lead lengths very short
Inductance Values are
5-10uH for low current
10-20uH for High current orient to avoid re-coupling