

CFP MSA 100G Roadmap and Applications

CFP MSA Member Companies:

Avago Technologies

Finisar Corp.

Fujitsu Optical Components

Opnext, Inc.

Sumitomo Electric Industries

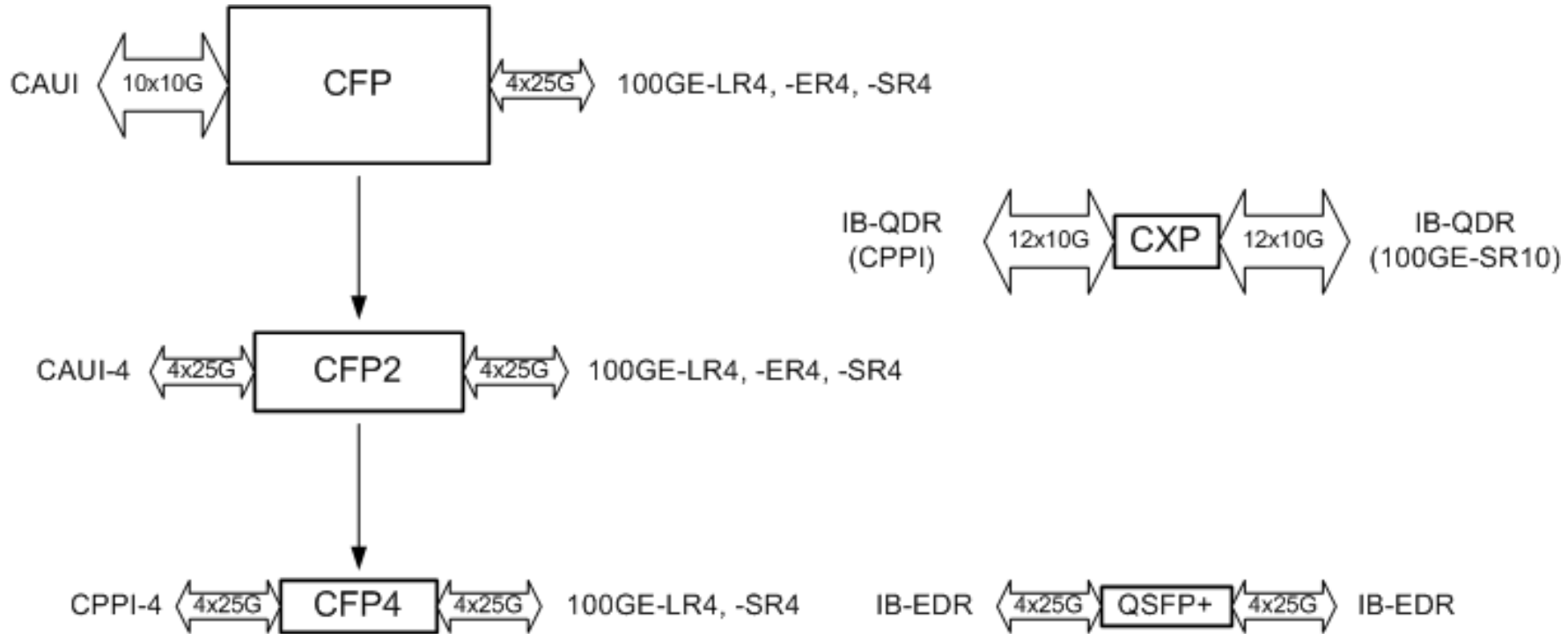
18 November 2010



Outline

- ❑ CFP MSA 100G Form Factor Roadmap
- ❑ CFP Application
- ❑ CFP2 Applications
- ❑ CFP4 Applications
- ❑ Appendix 1: Next Gen 100GE PMD
- ❑ Appendix 2: CFP2 & CFP4 40GE Applications

CFP MSA 100G Form Factor Roadmap



Module shapes all drawn approximately to same scale

- ❑ System OEMs have expressed reservations about jitter budget, reach, and thermal limitations of the 25G QSFP+ module
- ❑ CFP MSA will study CFP4 as alternative to QSFP+

CFP2 & CFP4 Feature Summary

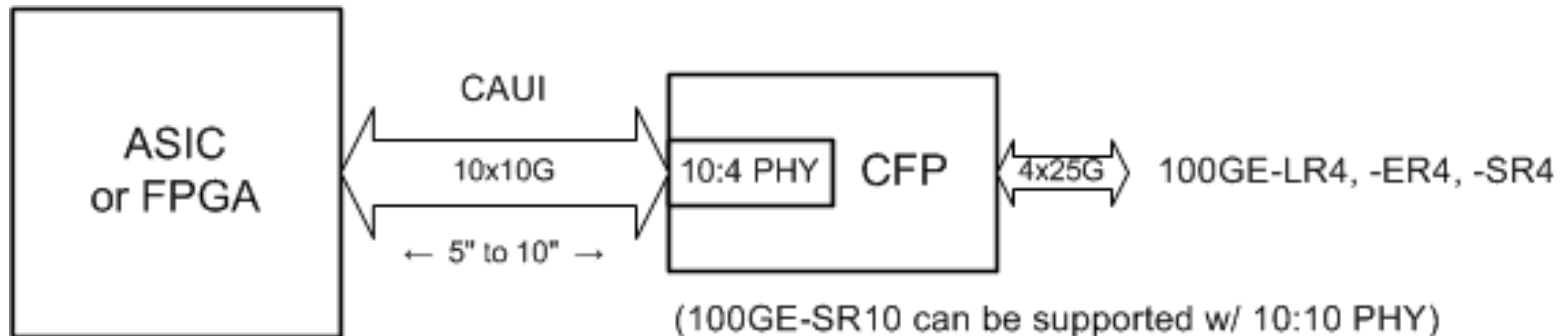
□ CFP2

- ~2x CFP faceplate density (exact dimensions TBD)
- 25G optimized top PCB layer only traces and connector pins
- 4W, 8W, 12W approximate power classes (exact pwr. TBD)

□ CFP4

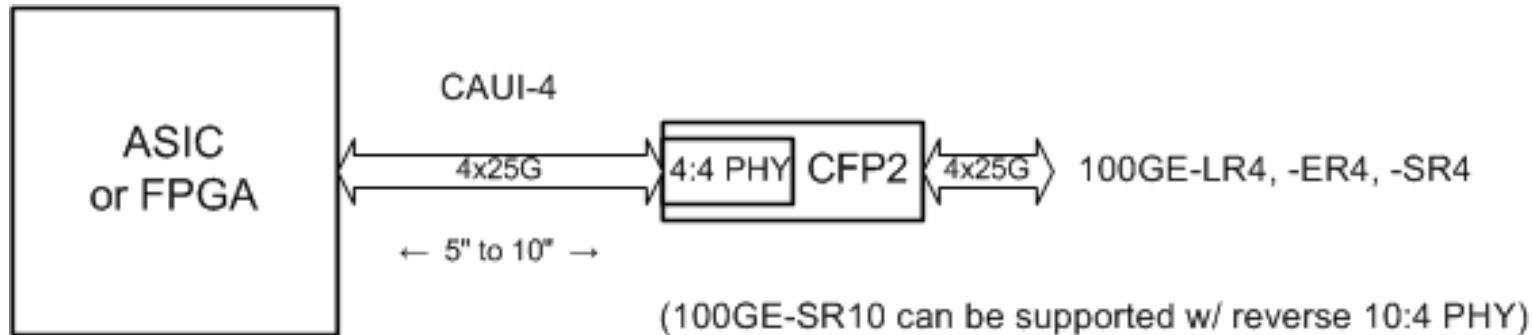
- ~4x CFP faceplate density (exact dimensions TBD)
- 25G optimized top PCB layer only traces and connector pins
- 2.5W, 5W approximate power classes (exact pwr. TBD)
- To enable higher power dissipation than QSFP+, CFP4 is slightly wider (no wider than CXP) and slightly longer

CFP Application



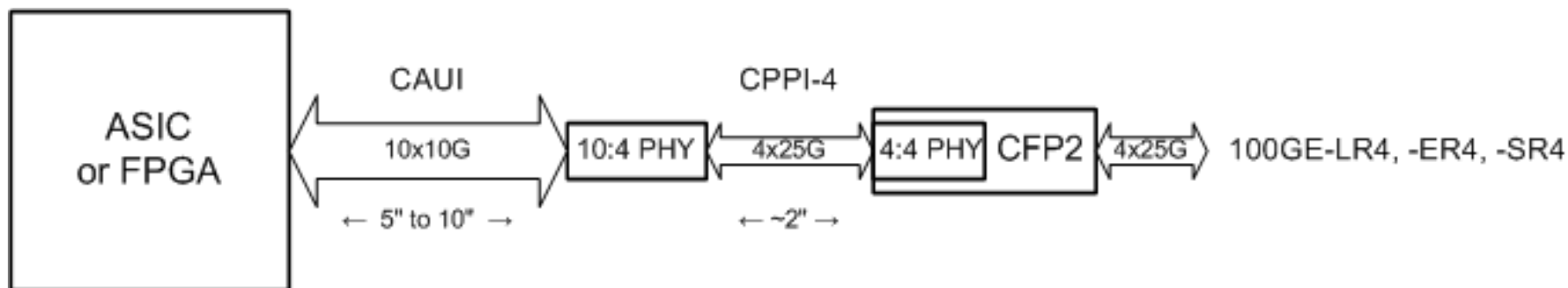
- ❑ CFPs today use SiGe 10:4 PHY which are only used for 100GE-LR4 and -ER4 applications
- ❑ CFP MSA module vendors will evaluate available future 10:4 PHY for use in reduced cost and power CFPs
- ❑ CFP module shipments started in 2010

CFP2 Application 1



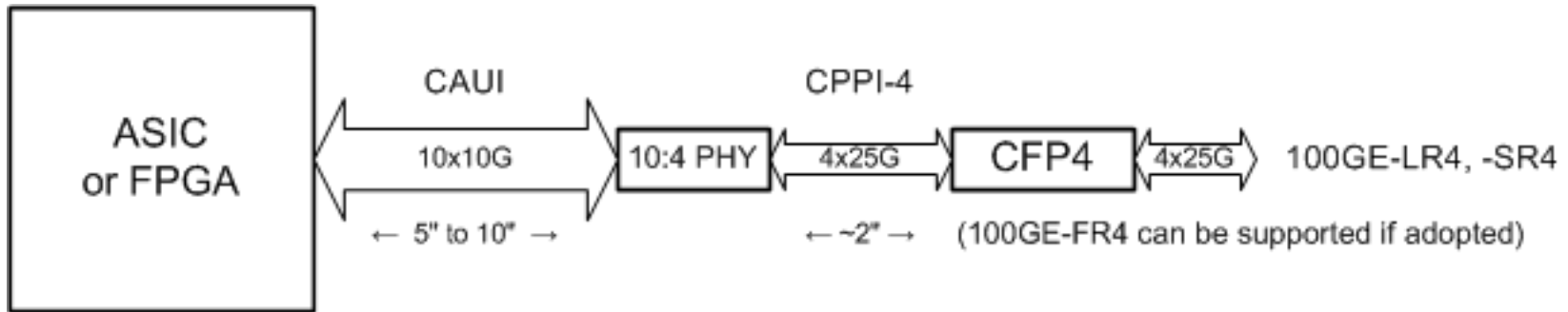
- ❑ Industry is discussing partnerships to develop host cards with multiple CFP2 ports
- ❑ Principal task is full 4x25G electrical interface simulation to enable first pass design success
- ❑ 4:4 PHY has to support higher power CAUI-4 mode
- ❑ CFP MSA module vendors will evaluate future available 4:4 PHY for use in CFP2
- ❑ CFP2 specification completion timeframe will enable 2012 product shipments

CFP2 Application 2



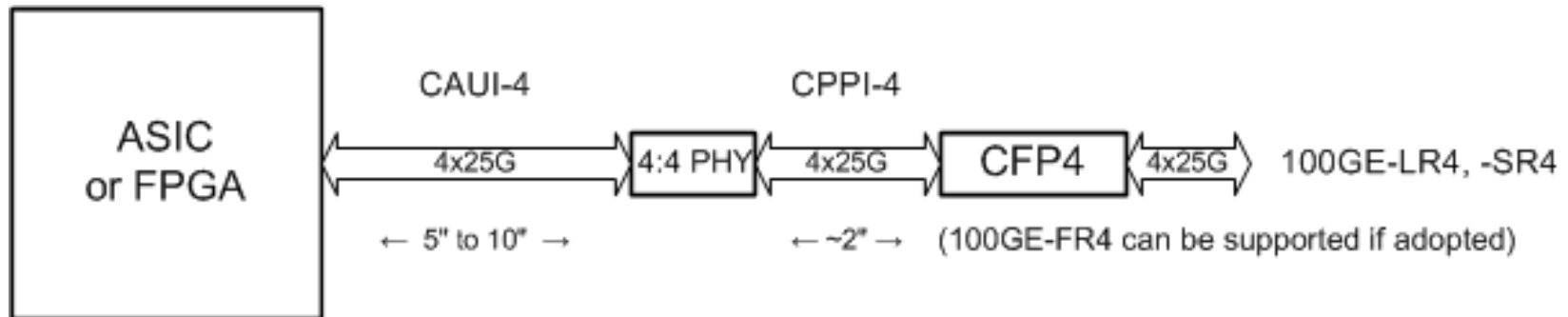
- ❑ Industry is discussing partnerships to develop host cards with multiple CFP2 ports
- ❑ Principal task is full 4x25G electrical interface simulation to enable first pass design success
- ❑ 4:4 PHY has to support lower power CPPI-4 mode
- ❑ CFP2 specification completion timeframe will enable 2012 product shipments

CFP4 Application 1



- ❑ Industry is discussing partnerships to develop host cards with high density CFP4 ports
- ❑ Principal task is full 4x25G end-to-end electrical and optical link simulation to enable first pass design success
- ❑ Second task is full card thermal simulation and design
- ❑ CFP4 specification completion timeframe will enable 2012/2013 product shipments

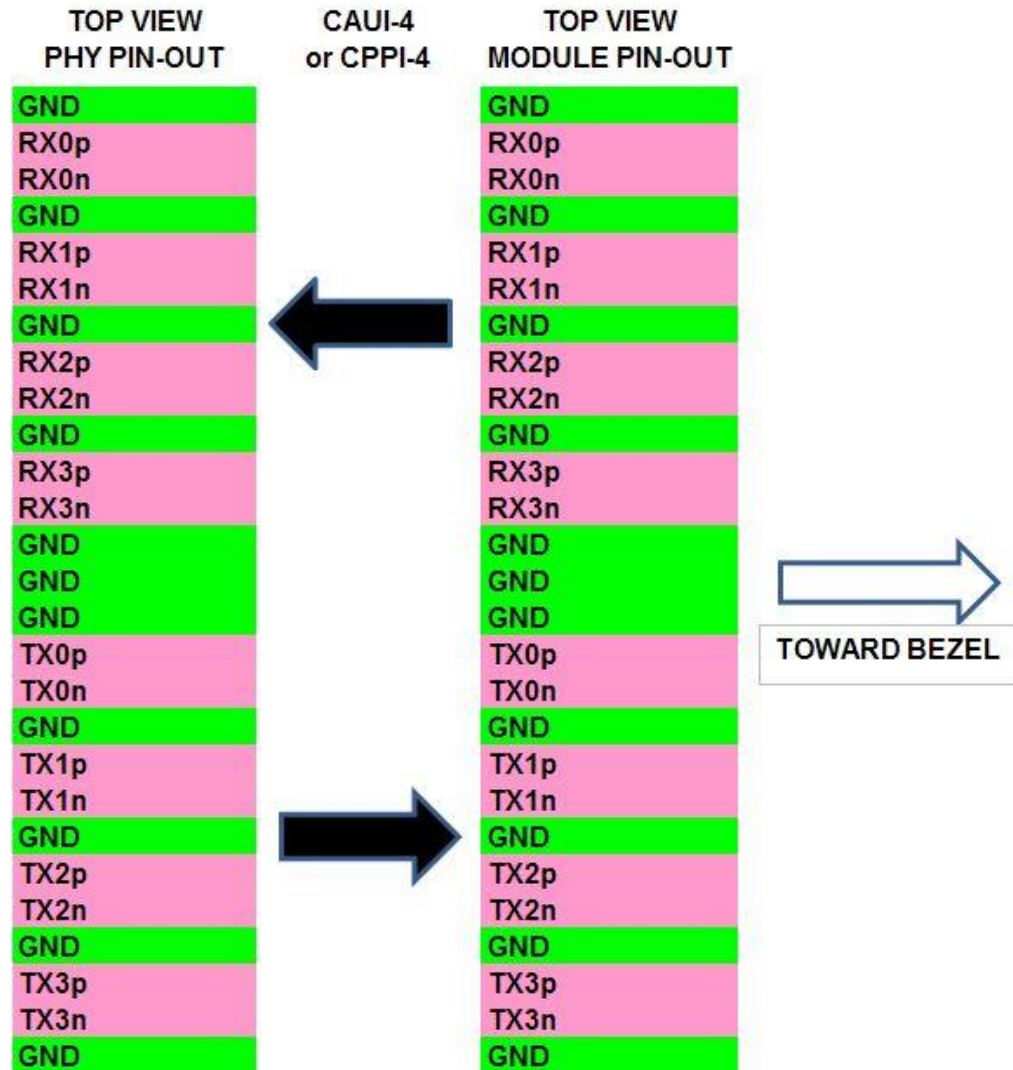
CFP4 Application 2



- ❑ Industry is discussing partnerships to develop host cards with high density CFP4 ports
- ❑ Principal task is full 4x25G end-to-end electrical and optical link simulation to enable first pass design success
- ❑ Second task is full card thermal simulation and design
- ❑ CFP4 specification completion timeframe will enable 2012/2013 product shipments

CFP2 & CFP4 Pin Ordering

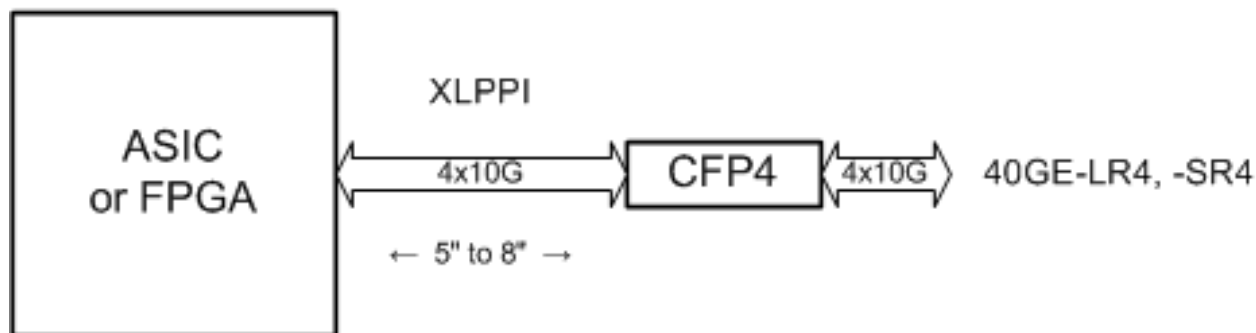
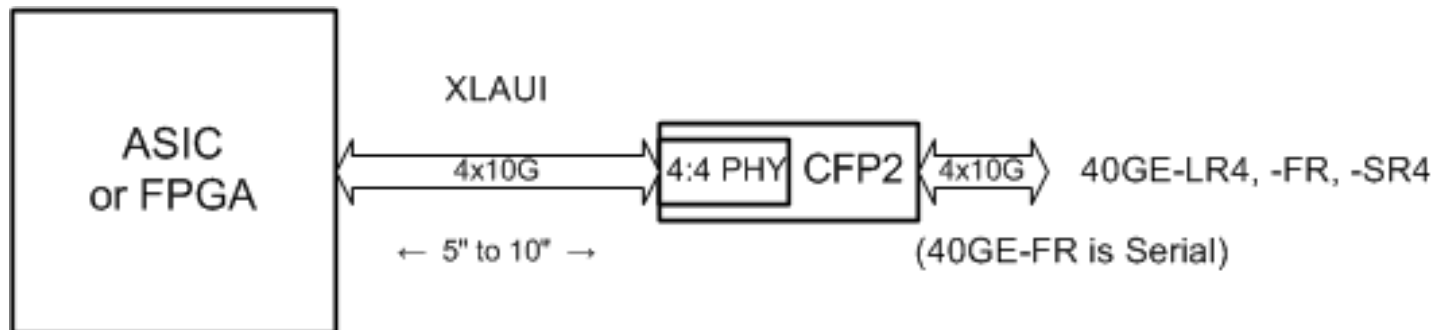
- ❑ CFP2 & CFP4 high speed pin ordering will be the same as CFP, which is the same as XAUI, SFI-5.2 & SFI-S
- ❑ CFP MSA recommends that PHY, ASIC and FPGA designers use the same pin ordering, so there is no need for host 25G trace crossover
- ❑ For cable applications, like 100GE-SR4 the module is pass through, with no trace crossover



Appendix 1: Next Gen 100GE PMD

- ❑ Proposed Next Gen 100GE IEEE 802.3 Study Group elements:
 - ❑ Short reach MMF PMD: 100GE-SR4
 - ❑ Possibly a new SMF PMD: 100GE-FR4
(need for this new PMD in addition to 100GE-LR4 to be determined)
 - ❑ CAUI-4
 - ❑ CPPI-4
(to be optimized for both SMF and MMF PMDs)
- ❑ CFI is likely in July'11
- ❑ 802.3 Next Gen PMD Study Group work should be based on proven technology, i.e. working solutions.
- ❑ 802.3 Next Gen PMD Study Group should coordinate with the 802.3 100Gb/s Backplane and Cu Study Group on 100GE-KR4 and 100GE-CR4 definitions

Appendix 2: 40GE Applications



- ❑ CFP2 and CFP4 will be defined to support 40GE applications
- ❑ Definition will be compatible with existing PHY, ASIC and FPGA ICs, with same pin-out ordering as CFP 40GE definition