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ACCELERATED PUBLICATION

Advanced PERC and PERL production cells with 20.3% record efficiency for standard commercial p-type silicon wafers

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ABSTRACT

Following intensive research and development, Suntech Power has successfully commercialised its Pluto technology with 0.5 GW annual production capacity, delivering up to 10% performance advantage over conventional screen-printed cells. The next generation of Pluto involves the development of improved rear surface design based on the design features of passivated emitter and rear locally diffused cells. Cells with an average efficiency over 20% were fabricated on 155 cm^2 commercial-grade p-type wafers using mass-manufacturing processes and equipment, with the highest single-cell efficiency independently confirmed at 20.3%. This is believed to be a record efficiency for this wafer type. Further optimisation work on contact pattern and rear surface passivation suggests the potential for further efficiency increase approaching 23%.

KEYWORDS
selective emitters; localised rear contact; silicon solar cells

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1. INTRODUCTION

Although screen-printed solar cell technology has dominated commercial manufacturing for the last 30 years [1], the worldwide photovoltaics industry constantly seeks to address performance limitations associated with the screen-printed front contacts, in an effort to achieve higher cell efficiencies. Among the emerging high-efficiency cell designs, the concept of the selective emitter appears to be the most eagerly pursued approach for commercial application in recent times [2]. Various innovative selective emitter technologies have been developed which have demonstrated an average efficiency of 18.5% in pilot or full-scale production [3–7].

Also employing the selective emitter concept is the Pluto cell technology developed by Suntech Power in collaboration with the University of New South Wales [8] based on the world-record holding passivated emitter and rear locally diffused (PERL) cell structure [9,10]. A schematic of Pluto cell is illustrated in Figure 1(a). By delivering aspects of PERL cells to improve the front surface design while retaining a full metal/silicon interface at the rear surface, Pluto achieves an average cell efficiency of ~19% in a 0.5 GW production, with highest efficiency of 19.6% independently confirmed [11,14]. This result translates to a 5–10% boost in efficiency, when directly compared with standard screen-printed cells (Table I).

Despite Pluto's superior performance over conventional screen-printed cells, device loss analysis of similar high-efficiency cell structures has indicated that the full metal/silicon interface at the rear surface accounts for over 50% of the total dark saturation current of the finished cell [12,13]. This finding clearly highlights the potential for

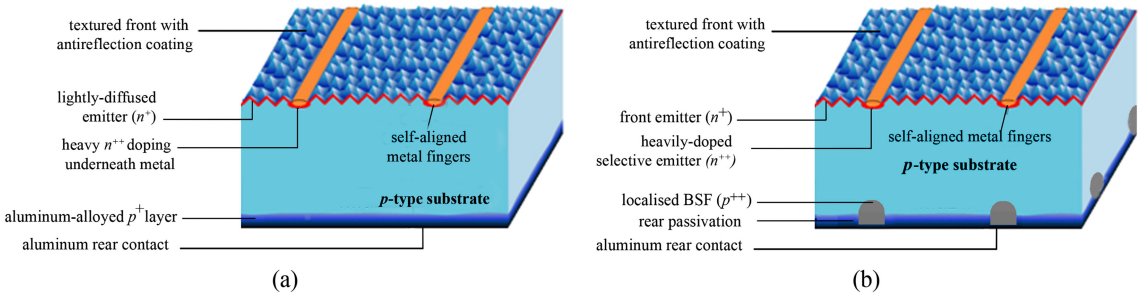

Figure 1. Schematic of (a) the first-generation Pluto cell with rear surface covered entirely with aluminium corresponding to 100% contact area for the metal/silicon interface surface [8] and (b) the next-generation Pluto cell with localised rear contacts.

Table I. Comparison of average cell performance from 0.5 GW Pluto production lines and an adjacent screen-printed line using large area p-type CZ wafers [11].

	V_{oc}	J_{sc}	FF	Eff
	(mV)	(mA/cm^2)	(%)	(%)
Screen-print	629	36.0	78.5	17.8
Pluto	632	38.2	78.8	19.0

further significant improvements in cell efficiencies. As part of the ongoing development of Pluto technology, changes and improvements to the rear surface design are currently being made by incorporating further attributes of PERL cells to address the abovementioned limitation (Figure 2). By doing so, the next generation of Pluto is expected to achieve well-over 20% efficiencies on commercial-grade p-type wafers.

In this paper, progress results on the development of next-generation Pluto technology are presented.

2. PROCESS FLOW OF PLUTO CELLS

Figure 2 depicts the evolution of Pluto technology during 5 years of research and development work. The key highlight of this transformation is the area reduction of the high-recombination metal/silicon interface at the rear surface, which significantly reduces the total dark saturation current J_0 within the device and therefore enables higher V_{oc} and J_{sc}.

As seen in Figure 2(b) and (c), the next generation of Pluto technology incorporates a standard plasma enhanced chemical vapour deposition (PECVD) SiN_x as a rear dielectric layer to replace the simultaneously formed aluminium-doped back surface field (BSF) and rear contacts of a conventional Pluto cell. Localised openings are created in the SiN_x dielectric to provide mechanisms for contacting the bulk silicon. The opening coverage defines the total metal/silicon interface area and hence is kept to a minimum to be just sufficient for current collection.

The next-generation Pluto technology undergoes two evolutionary stages of development in device structure. The first stage employs the design concept of passivated emitter and rear cell (PERC), whereby the localised rear openings are left undoped prior to rear surface metallisation (Figure 2 (b)). In the second stage, a heavy p^{++} boron diffusion is introduced into the rear silicon openings to produce a localised BSF, similar to that of PERL cell structure (Figure 2(c)).

The next generation of Pluto also minimises the use of high-temperature processes, which makes it suitable to be implemented on the most commonly used commercial wafer types used by the industry. In substitution of screen-printed contacts, sputtered aluminium is used for rear contact formation because of its ability to be sintered at low temperature to form ohmic contacts, whereas self-aligned plated metallisation comprising more than 90% copper is used for the front contacting scheme.

3. ONGOING DEVELOPMENT OF HIGH-PERFORMANCE PLUTO TECHNOLOGY

3.1. Device fabrication

The Pluto technology utilises 155 cm^2 p-type commercial-grade CZ wafers, with bulk resistivity of 1–3 Ω cm and wafer thickness of 180 μm after texturing. The next generation of Pluto cells that encompasses Pluto-PERC and Pluto-PERL were fabricated on the basis of the process flow outlined in Figure 2(b) and (c). The patterned rear SiN_x dielectric layers consist of line openings with 2 mm and 1 mm spacings for Pluto-PERC and Pluto-PERL, respectively.

The finished cells were characterised using the light J-V, Suns-V_{oc} and spectral response measurements. To further study the device properties, fitting to the cell's internal quantum efficiency (IQE) curve was attempted in PC1D to extract relevant device parameters, such as bulk lifetime and surface recombination velocity (SRV).

3.2. Results and discussion

3.2.1. High-efficiency features in the next-generation Pluto

As seen in Table II, despite its early stage of development, the next-generation Pluto is already producing

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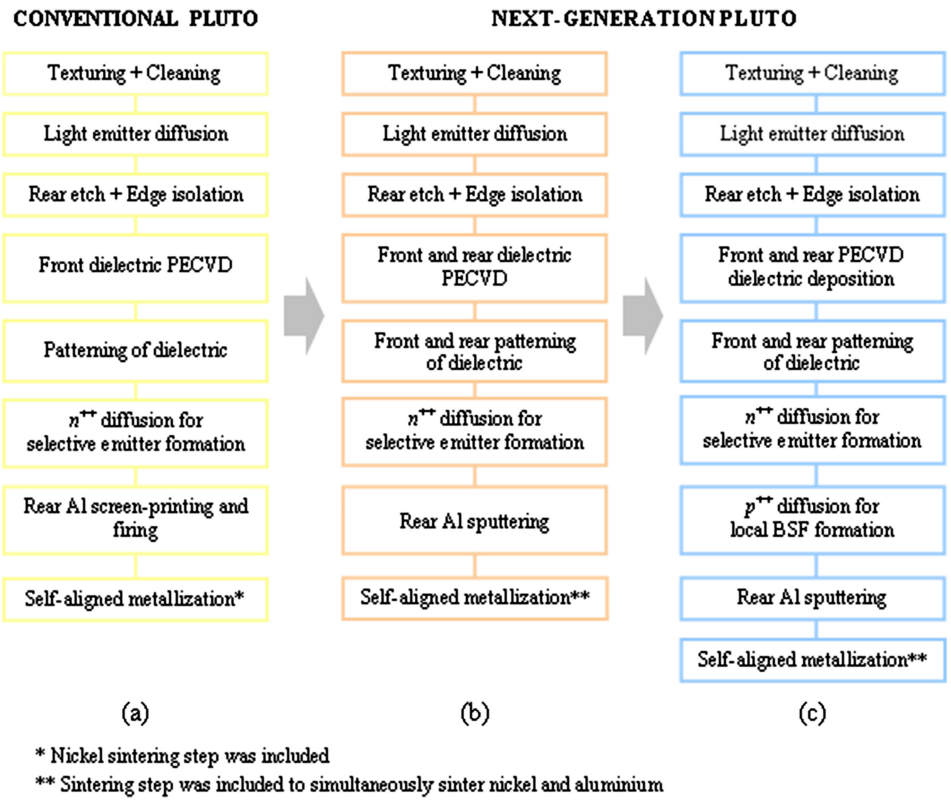

Figure 2. Process flow diagram for (a) first-generation of Pluto cell [8], (b) next-generation Pluto cell based on passivated emitter and rear cell rear surface design (Pluto-PERC), and (c) next-generation Pluto cell based on passivated emitter and rear locally diffused rear surface design (Pluto-PERL).

Table II. Light J-V and average Suns-V_{oc} data of next-generation Pluto cells.

	Light J-V measurement				Suns-V_{oc} measurement			
	V_{oc}	J_{sc}	FF	Eff	pFF	*n* at	J_{01}	J_{02}
	(mV)	(mA/cm^2)	(%)	(%)	(%)	1-Sun	(pA/cm^2)	(nA/cm^2)
Pluto [11,14]								
Best cell*	**636**	**38.6**	**79.7**	**19.6**	—	—	—	—
Average	632	38.2	78.8	19.0	82.8	1.02	0.72	8.25
Pluto-PERC								
Best cell*	**674**	**39.3**	**73.9**	**19.7**	—	—	—	—
Highest V_{oc}	683	39.3	72.1	19.4	—	—	—	—
Average	674	39.0	73.6	19.3	81.1	1.12	0.148	24.0
Pluto-PERL								
Best cell*	**665**	**40.9**	**74.4**	**20.3**	—	—	—	—
Highest V_{oc}	668	40.5	73.3	19.9	—	—	—	—
Average	662	40.7	74.3	20.2	83.3	1.06	0.151	21.2

Data for conventional Pluto cells were extracted from Ref. 11 and 14 and included for comparison. The bold emphasis is to highlight the best cell efficiency results from each group.

PERC, passivated emitter and rear cell; PERL, passivated emitter and rear locally diffused.

*independently measured by Solar Energy Research Institute of Singapore.

average cell efficiencies of more than 1% absolute above those achieved by the conventional Pluto technology. Late 2010, the best conventional Pluto cell was independently confirmed by the Solar Energy Research Institute of Singapore (SERIS) to be 19.6% in efficiency, representing a record efficiency for standard commercial p-type wafers. Earlier in 2011, a new record of 19.7% [14] was independently confirmed by SERIS for a Pluto cell using

the Pluto-PERC cell structure and the same commercial p-type wafers. More recently, an efficiency of 20.3% has again been independently confirmed by SERIS on similar commercial-grade wafers, this time using the Pluto-PERL structure.

The efficiency boost demonstrated by the next-generation Pluto is primarily attributed to the improved rear surface design that leads to up to 6% higher V_{oc} and J_{sc}. As listed in Table III, the next-generation Pluto cells demonstrated a significant reduction in rear SRV approaching four orders of magnitude, which indicates the effectiveness of the rear SiN_x dielectric layer in passivating the p-type surface while restricting the metal/silicon interface area to less than 2% of the rear surface.

The reduction in rear SRV is also accompanied by a reduced bulk recombination to maximise the voltage increase. The next generation of Pluto cells was shown to exhibit improved bulk lifetime over conventional Pluto cells by a factor of five, from 100 to 500 µs (Table III). As both conventional Pluto and next-generation Pluto use similar quality, resistivity and thickness of CZ wafers, the significant increase in bulk lifetime is made possible by the use of a PECVD hydrogenation process at 400 °C and the subsequent avoidance of temperatures above 400 °C when forming the metal contacts. In a separate work, attempts to introduce similar hydrogenation processes into the screen-printed cells were unsuccessful, with bulk minority carrier lifetimes falling by more than an order of magnitude from almost 1 ms to ~60 µs during the high-temperature firing of the screen-printed contacts.

The improved bulk lifetime through hydrogenation demonstrated in this work is a particularly important finding given that the International Technology Roadmap for Photovoltaics in relation to screen-printed cell technology for the next 10 years only targets the achievement of 20% efficiency [16]. Such a projected efficiency target is reasonable given the present expectation of commercial p-type wafers being limited in bulk minority carrier lifetimes to below 100 µs. In comparison, the high bulk minority carrier lifetimes approaching 1 ms combined with the Pluto-PERL cell structure lead to radically different conclusions as to the achievable production cell efficiencies with 23% eventually likely (see Section 4.2).

Table III. Simulated light J-V data and relevant device parameters for Pluto cells in Figure 3 based on the fitting of the measured internal quantum efficiency curve and light J-V data.

	Pluto	Pluto-PERC	Pluto-PERL
Device parameters			
Emitter sheet resistance (Ω/)	100	140	140
Bulk lifetime (µs)	100	500	500
Front SRV (cm/s)	1000	1000	1000
Rear SRV (cm/s)	1×10^6	180	100
Rear series resistance ($\Omega\,cm^2$)	1×10^{-6}	1.4	1.1
Simulated J-V results			
V_{oc} (mV)	636	670	666
J_{sc} (mA/cm2)	38.6	39.7	40.6
FF (%)	79.8	73.6	74.3
Efficiency (%)	19.6	19.6	20.1

PERC, passivated emitter and rear cell; PERL, passivated emitter and rear locally diffused.

In addition to rear surface and bulk recombination, other sources of recombination such as the n^+ emitter and front SRV were investigated. In the attempt to minimise emitter recombination, the next-generation Pluto cells use a slightly higher emitter sheet resistance of ~140 Ω/□, which contributes to an additional 5–10 mV increase in V_{oc} as modelled in PC1D (Table III). As shown in Table III, the front SRV values however remain similar at 1000 cm/s as expected with both implementations using the same front surface design. The IQE curves in Figure 3 confirm that the front surface design has been adequately optimised as the IQE values at short wavelengths are close to unity for all cells.

All of the abovementioned improvements resulted in a total of 30–40 mV increase in V_{oc}, with a large proportion of the increase being contributed by improved rear surface passivation and bulk lifetime. Device's V_{oc} as high as 683 mV (Table II) has been demonstrated. A corresponding improvement in J_{sc} of ~0.5 mA/cm^2 was estimated by PC1D, to have followed from the described improvements that lead to the improved V_{oc}.

The remaining increase in J_{sc} originates from the high internal reflectance provided by the rear SiN_x dielectric and aluminium sputtered rear that acts as a rear reflector. As depicted in Figure 4, the reflectance of next-generation Pluto cells is as high as 65% at 1200 nm wavelength, which is significantly higher than that of conventional Pluto with only 25%. Such a high reflectance is beneficial such that the long wavelengths of light do not easily escape from the rear surface nor are significantly absorbed during internal reflection from the rear metal. Instead, such infrared light is reflected into the solar cell for further absorption within active regions of the device. This cell property, along with well-passivated rear surface, translates to superior IQE for $\lambda > 900$ nm, indicating increased carrier collection at long wavelengths.

3.2.2. Comparison of Pluto-passivated emitter and rear cell and passivated emitter and rear locally diffused

Although the next-generation Pluto outperforms the conventional Pluto, Pluto-PERL produced higher performance cells than Pluto-PERC by 1% absolute efficiency on average. As seen in Table II, the main contributor to such higher efficiencies is the superior J_{sc} values of Pluto-PERL close to 41 mA/cm^2 because of lower rear SRV and higher internal reflectance from the rear metal/dielectric configuration.

Pluto-PERL was found to benefit from a lower rear SRV than Pluto-PERC approximately by a factor of two (Table III). The heavily doped p^+ regions at the rear side of Pluto-PERL act as a localised BSF that isolates minority carriers from the high-recombination metal/silicon

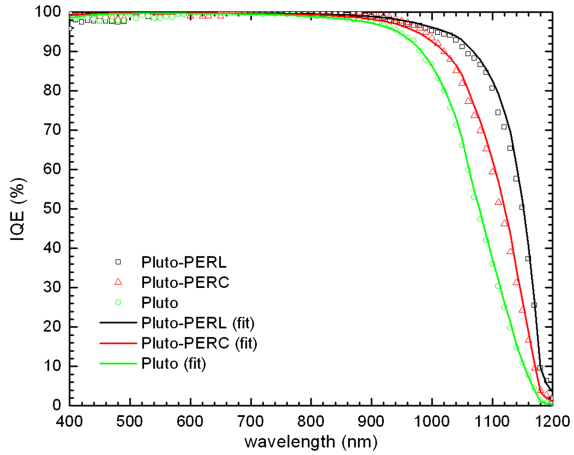

Figure 3. Internal quantum efficiency (IQE) curves of the best Pluto-passivated emitter and rear cell (PERC) and Pluto-passivated emitter and rear locally diffused (PERL) cells and the attempted curve fit by PC1D. IQE data for conventional Pluto cells were extracted from Ref. 11 and included for comparison.

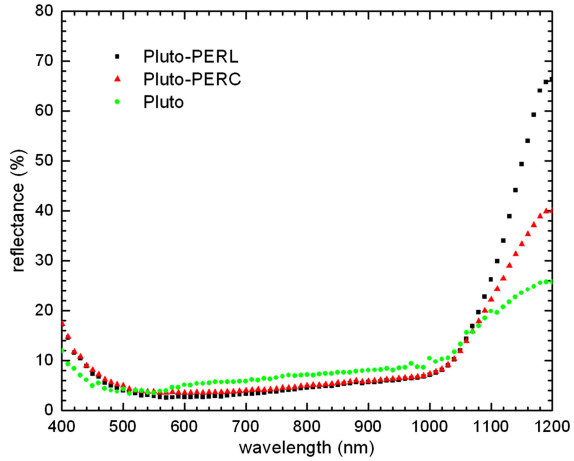

Figure 4. Corresponding reflectance curves of the next-generation Pluto cells in Figure 3. Reflectance data for conventional Pluto cells were extracted from Ref. 8 and included for comparison.

interface, resulting in an overall lower effective rear SRV and hence higher generated current. The presence of the p^+ regions is confirmed by Figure 5, whereby a significantly higher p-type dopant concentration is observed for Pluto-PERL. In the Pluto-PERC cell, a more lightly doped p^+ region is evident in the vicinity of the rear metal/silicon interface. This was formed by heating the sputtered aluminium to a temperature marginally above the aluminium-silicon eutectic temperature of 577 °C with the subsequent liquid phase epitaxial regrowth of the silicon during cooling leading to the aluminium doping of the silicon at its solid solubility for the temperatures involved.

As seen in Figure 4, Pluto-PERL introduces 65% reflectance at 1200 nm wavelength while Pluto-PERC only reflects 40% at similar wavelength. This appears to be due to reduced absorption in the rear metal as the lower aluminium sintering temperature at ~350 °C provides superior reflection properties. The high internal reflectance increases absorption of long wavelengths of light and enhances carrier collection in the vicinity of the rear surface, as depicted by the spectral response curve in Figure 3.

In addition to a higher J_{sc}, Pluto-PERL also yields a higher fill factor (FF) that contributes to the higher efficiency results. As seen in the doping profile shown in Figure 5, the localised p^+ regions in Pluto-PERL introduces a significantly higher doping concentration at the silicon surface that is beneficial for facilitating a lower contact resistance of the p-type contacts. Furthermore, Pluto-PERL utilises a smaller rear-contact spacing which decreases series resistance losses in the substrate.

It can be seen from Table II that the FF values demonstrated by both Pluto-PERC and Pluto PERL are still fairly low. The high pseudo FFs (pFF) >81% for both types of cell show that there is minimal shunting or junction recombination present in the devices, and therefore the dominant loss mechanism for the device's FF lies in the parasitic

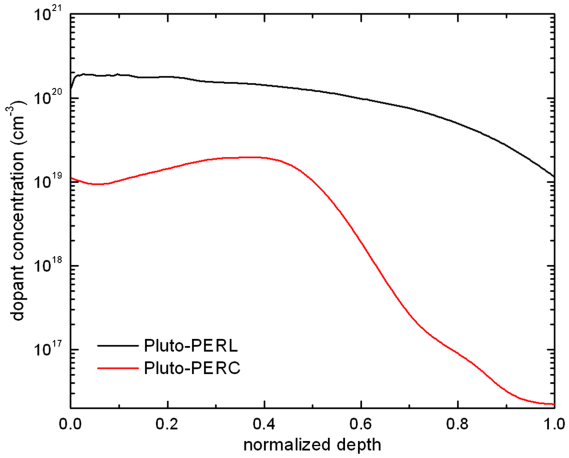

Figure 5. Electrochemical capacitance voltage doping profile of the rear p-type silicon opening for Pluto-passivated emitter and rear cell (PERC) and passivated emitter and rear locally diffused (PERL) cells. The depths of the p^+ regions are normalised to that of Pluto-PERC.

series resistance. From PC1D modelling, the series resistance of the rear contact for both Pluto-PERC and Pluto PERL is 1 Ω cm^2, which is reasonably high compared with a typical full rear aluminium contact on a conventional Pluto cell (Table III).

The V_{oc} of Pluto-PERL was found to be lower than Pluto-PERC by ~10 mV (Table II). Although the presence of the localised BSF reduces recombination at the rear surface, Pluto-PERL has the heavily boron-doped silicon and corresponding increased percentage of metal/silicon interface area which is not passivated by the SiN_x dielectric layer. This appears to outweigh the potential V_{oc} increase resulting from reduced rear SRV.

4. PC1D MODELLING: POTENTIAL IMPROVEMENTS IN PLUTO CELL EFFICIENCY

4.1. Rear surface and bulk recombination

As discussed in Section 3.2.1, reductions in rear surface and bulk recombination accounted for the majority of the V_{oc} improvement in the next-generation Pluto technology. In this section, PC1D simulations were performed on the basis of the 20.3%-efficient Pluto-PERL cell parameters, to quantify the efficiency improvements through further reductions in device's rear surface and bulk recombination. Figures 6 and 7 summarise the interrelated impact of bulk lifetime, wafer thickness and rear SRV on cell efficiency.

As seen in Figures 6 and 7, a further 1% absolute increase in efficiency can be potentially achieved through reduction in rear SRV by at least an order of magnitude from 100 to 10 cm/s. As part of the ongoing development of the Pluto technology, such a low rear SRV can be made possible through the use of a standard PECVD SiN_x passivation.

In Pluto-PERL, further increases in bulk lifetime have been demonstrated on test devices through improved hydrogenation with minority carrier lifetimes over 1 ms (unpublished work). However, as shown in Figure 6, an increase in bulk lifetime alone from 500 to 1000 µs only results in a 0.1% higher efficiency for SRV = 100 cm/s. Such a small efficiency increase is primarily because the J_0 contribution from the wafer is already having minimal impact on the total device's J_0. In addition, the corresponding minority carrier diffusion lengths are already sufficiently long to collect carriers from any regions within the device, with recombination at the rear surface providing the primary limitation to collection of carriers generated close to the rear surface. The improved bulk lifetimes are therefore only of benefit to the efficiency if accompanied by a reduction in rear SRV values.

In addition to improved bulk lifetime, bulk recombination can also be effectively reduced through the use of thinner wafers. However, Figure 7 shows that for a bulk lifetime of 500 µs, thinner wafers result in lower cell efficiencies. Decreasing wafer thickness generally results in decreases in the cell efficiency because of reduced absorption for medium to long wavelengths of light, particularly because the current Pluto-PERL cell design does not incorporate enhanced light-trapping schemes. This result highlights that the current bulk lifetime of 500 µs is sufficiently high as to not dominate the total recombination within the device and limit the cell's V_{oc}. In this case, the use of thinner wafers is therefore not recommended. From Figure 7, it was found that the ideal wafer thickness for Pluto-PERL is ≥150 µm to achieve maximum cell efficiency.

4.2. Series resistance

One of the major limiting factors that currently prevents Pluto-PERL cells from achieving higher efficiencies was identified to be the high series resistance at the rear p-type contacts. Considering the high p-type doping concentration at the metal/silicon interface to ensure low contact resistance shown in Figure 5, the high series resistance is likely to be

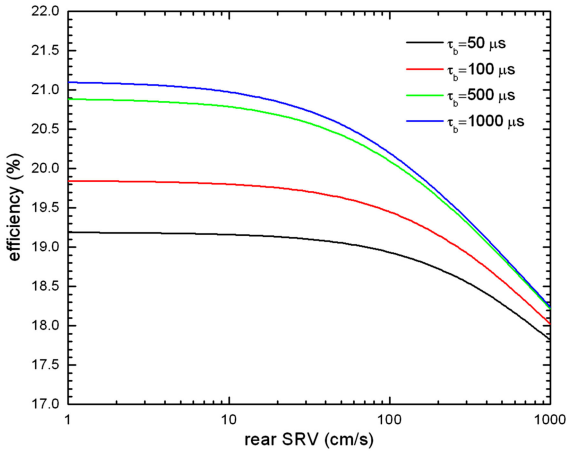

Figure 6. Simulated efficiency results for varying rear surface recombination velocity (SRV) and bulk lifetime based on the device parameters of the best Pluto-passivated emitter and rear cell listed in Table III. The wafer thickness is set to 180 μm.

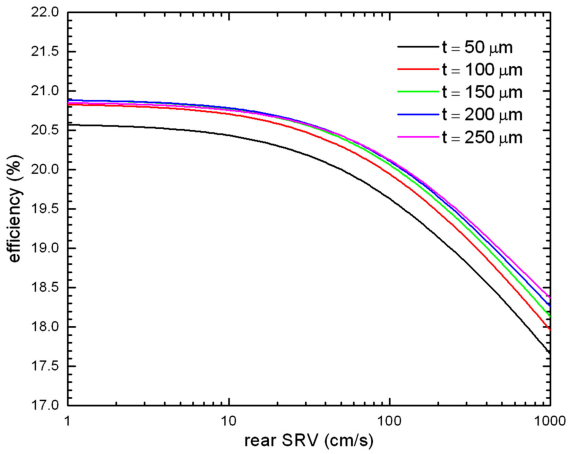

Figure 7. Simulated efficiency results for varying rear surface recombination velocity (SRV) and wafer thickness based on the device parameters of the best Pluto-passivated emitter and rear cell listed in Table III. The bulk lifetime is set to 500 μs.

caused by non-optimum emitter sheet resistance and/or ineffective carrier collection given by the existing contact pattern.

The impact of the emitter sheet resistance values on cell efficiency were investigated using PC1D simulations based on the 20.3%-efficient Pluto-PERL cell parameters. The cell efficiency was calculated after taking into account the lateral resistance losses in the emitter according to the following equation [15]:

$$P_{\mathrm{em}} = \frac{\rho_{\mathrm{s}}}{12} \times \frac{J_{\mathrm{mp}}}{V_{\mathrm{mp}}} \times S^2$$

where P_{em} = fractional power loss because of emitter resistivity; ρ_{s} = emitter sheet resistance (Ω/□); J_{mp} = current at maximum power point (mA/cm^2); V_{mp} = voltage at maximum power point (mV); S = finger spacing of front contacts (cm).

It can be seen from the black curve in Figure 8 that the current sheet resistance of 140 Ω/ does not introduce significant resistive losses that limit the device's FF. In general, the fractional power loss because of emitter resistivity for Pluto cells is reasonably small primarily because of narrow finger spacings of the front metal contacts (~1 mm) [11]. In fact, high emitter sheet resistances are preferred for Pluto-PERL structure to reduce the emitter recombination. From Figure 8, the optimum sheet resistance ranges from 120 to 200 Ω/□ where a balance between emitter recombination and low series resistance is achieved. However, in practice, sheet resistance values ≥150 Ω/□ often results in FF degradation because of metal puncturing through the (shallow) junction during front contact metallisation.

On the basis of the results of the emitter sheet resistance investigation in Figure 8, it can be deduced that the high series resistance is likely to be caused by a non-optimised wafer resistivity and rear contact design for carrier collection. Optimisations of the contact pattern can be realised

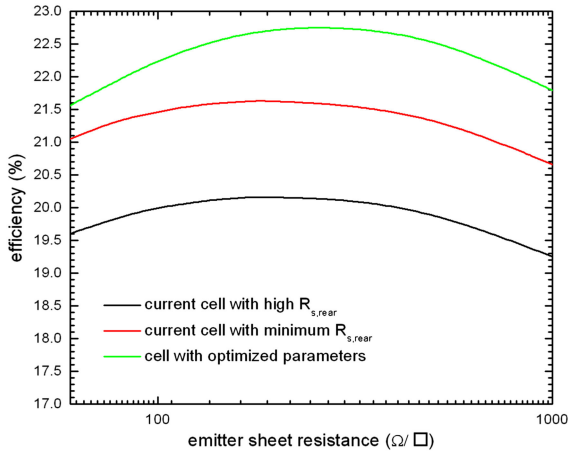

Figure 8. Simulated efficiency results for varying emitter sheet resistance for current cell with $R_{s,rear} = 1.1\,\Omega\,cm^2$ (black line); current cell with $R_{s,rear} = 0.1\,\Omega\,cm^2$ (red line); and cell with $R_{s,rear} = 0.1\,\Omega\,cm^2$, $500 \le \tau_b \le 1000\,\mu s$, rear surface recombination velocity = 10 cm/s (green line). The term 'current cell' refers to the 20.3% passivated emitter and rear locally diffused cell with device parameters listed in Table III unless stated otherwise. From PC1D modelling, an $R_{s,rear} = 0.1\,\Omega\,cm^2$ corresponds to a fill factor of 80%.

through the use of point contacts, which enables the p-type metal/silicon interfaces to be spaced closer to lower resistive losses while maintaining the same percentage of metal coverage of ~1%. The unnecessarily high wafer minority carrier lifetimes also suggest that lower wafer resistivities could be beneficially used to reduce series resistance, with minimal impact on either current collection or open-circuit voltage. However, it is important to note that the lower wafer resistivity could potentially cause deterioration in the rear SRV. PC1D simulation predicts that a cell efficiency of 21.5% can be achieved by solving the series resistance issue alone (red curve in Figure 8). Furthermore, as the rear SRV is reduced down to 10 cm/s, the next generation of Pluto technology is estimated to reach cell efficiency as high as 22.7%.

5. CONCLUSION

In this paper, progress results on the development of next generation of Pluto technology were reported. In the next generation of Pluto, high-efficiency features of PERL cells were incorporated to improve the rear surface design of conventional Pluto cell, primarily by reducing the metal/silicon interface area while keeping the remaining non-contacted area well-passivated.

To date, more than a 1% absolute increase in average efficiency has been achieved over conventional Pluto cells. The high average pFF of 83.3% and n nearing unity indicate that minimal shunting or junction recombination is present. Best efficiency of 20.3% was successfully demonstrated on standard commercial-grade p-type wafers, with a rear SRV as low as 100 cm/s and an improved bulk lifetime as high as 500 µs.

Device loss analysis of the best Pluto cell revealed that significant further improvements in cell efficiency can be achieved by addressing the series resistance issue and further reducing the rear SRV to produce higher FF and V_{oc}, respectively. The next stage of Pluto development therefore focuses on the implementation of a rear point-contact pattern to minimise series resistance while keeping the percentage of the metal/silicon area to ~1%. This appears likely to lead to efficiencies of at least 21.5%, which when combined with expected further improvement in rear surface passivation, could take corresponding cell efficiencies to approaching 23%.

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