FRONT GRID DESIGN FOR PLATED CONTACT SOLAR CELLS

U.Gangopadhyay¹, H.Saha², S.K.Dutta², Kyunghae Kim,¹ K.Chakrabarty,³ and Junsin Yi¹ ¹School of Electrical and Computer Engineering, Sungkyunkwan University 300 Cheoncheon Dong, Jangan-gu, Suwon, South Korea (440-746) E-mail: yi@yurim.skku.ac.kr ²IC Design and Fabrication Centre, Electronics and Tele-communication Engineering Department Jadavpur University, Kolkata-700032, India, E-mail: juicc@vsnl.com ³ Photon Semiconductor and Energy Company 300 Cheoncheon Dong, Jangan-gu, Suwon, South Korea (440-746)

ABSTRACT

Front grid pattern of standard crystalline solar cells is specifically designed for screen printed silver paste contact. A detailed theoretical analysis of the proposed segmented cross grid line pattern has been carried out for optimizing the spacing and widths of the grid finger, main and sub-bus bars. It is shown that by choosing properly the grid pattern and optimizing the grid parameter, the overall front contact electrical and optical losses can be brought down to 10% or less as compared to the usual loss of 15% or more obtained with the conventional screen printed silver paste technology. Limitation of conventional screen printed contact has been pointed out. It was also observed that the total normalized power loss for segmented mesh grid with plated metal contact, the total power loss can be brought down to 10.04 percent unlike 11.57 for the case of continuous grid and plated contact.

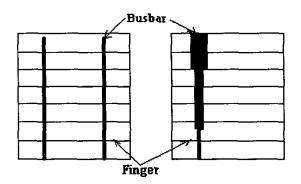
INTRODUCTION

One important area of cell design is the design of the top grid metal contact [1-3]. This area becomes increasingly important as the size of the individual cells increases. The grid pattern needs to be modified, for plated metal to improve efficiency of solar cells. The front contact grid pattern for 10cm×10cm square crystalline silicon solar cell of has been designed by optimization of two contradictory criteria, (a) minimizing the resistive loss by increasing the width and height of grid lines and bus bars as well as increasing the numbers of grid lines, (b) minimizing the optical losses by decreasing the width and number of grid lines and bus bars. The electrical loss further depends on the specific sheet resistance of the grid lines and bus bars, diffused emitter layer β as well as on the voltage and current density at maximum power point.

In this paper, two grid patterns have been proposed for 10cm×10cm square mono-crystalline silicon solar cells, and detailed theoretical analysis of the proposed segmented cross grid line pattern has been carried out for optimizing the spacing and widths of the grid finger, main and sub bus bars.

GRID PATTERN

Fig. 1 shows typical front grid patterns. Two types of metal lines can be identified namely (i) bus bars (i) fingers. The different front contacts are usually designed depending on the shape, size of the front surface, the specific sheet resistances of the emitter layer, metal used, and also the electrical parameters (J_{mp} , v_{mp}) of the cell. However, as we shall see that in many cases, the actual grid pattern may be dictated by the limitations of the technical process through which the grid metallization schemes are realized in practice.



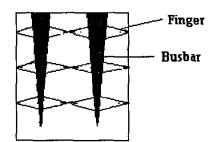


Fig.1 Different grid contact patterns

MODEL DESCRIPTION

A symmetrical grid pattern scheme consisting of two uniform bus bars and equally spaced uniform fingers is shown in fig.2. The maximum power output of a cell is JmpVmpAB, where AB is the area of the cell, Jmp and Vmp are respectively the current density and voltage at the maximum power point.



Fig.2 Two uniform bus bar and equally spaced continuous grid pattern

The electrical and optical power losses normalized to the maximum output of the cell (fractional losses) can be calculated to give the following results

Resistive power losses :

a) Fractional resistive power loss due to lateral current flow in the emitter layer = $p_{t1} = (1/12)p_s S^2 (J_{mp}/V_{mp})$ Where ps is Sheet resistivity of the emitter layer and S is the Pitch of the fingers

b) Fractional resistive power loss in the fingers

 $= p_{rf} = (1/3) p_{smf} (S/W_f) b_1^2 (J_{mp}/V_{mp})$

=(1/3) $\rho_{smf}(S/W_{f})[(B/2-W_{b})/2]^{2}(J_{mp}/V_{mp})$ Where b₁ = length of each current collecting finger on either side of the bus bar.

W_b = Width of bus bar.

c) Fractional resistive power loss due to contact resistance $P_{cf} = \rho_c(S/W_f)(J_{mp}/V_{mp})$, Where $\rho_c = Specific contact$

resistance of the metal with silicon in Ohm.cm². d) Fractional resistive power loss in the bus bars

 $p_{rb} = (2/3)A^2b_1 (\rho_{smb}/W_b)(J_{mb}/V_{mb}),$

Where parts= Sheet resistivity of the bus bars.

Optical power losses :

a) Fractional optical power loss in the finger=psf = W/S b) Fractional optical power loss in the bus bars

= p_{sb}=w_b/(B/2)≈w_b/2b₁

The total fractional power loss will then be given by

p = pres + Popt

= (p_{t1}+p_{cf}+p_{rf}+p_{rb}) + (p_{sf} + p_{sb})

It can be observed that except prb and psb , other losses do not have any dependence on wb. Therefore, the power loss due to bus bar can be optimized independently and it occurs when the optical loss in the bus bar equals its resistive loss and the optimized W_b is given by

 $W_{b}=2Ab_{1}\sqrt{(((1/3)\rho_{mb})/(J_{mp})/(J_{mp}))}$

The optimization of finger spacing (S) and finger width (W) will be more complex. The optimization will occur when S→0 and simultaneously

 $W_f/S = \sqrt{[(1/3)\rho_{sm}b_1^2 + \rho_c]}(J_{mp}/V_{mp})$

With these considerations , we can calculate the optimum values of W₆, W₇ and S for optimum performance of the cells. It can, however, be easily seen that lower and lower S and simultaneously lower value of W will produce lower losses.

However, each of the grid formation technologies has its own limitation on how small W and S can be made and therefore the adopted technology sets the limit for minimum losses.

Therefore, we have calculated numerically, the losses for the screen printed contacts, which are mostly used for commercial silicon solar cells.

Experimental:

The contact pattern was formed by printing silver paste through the openings in a screen on to the wafer. A good electrical and mechanical contact was obtained after drying and firing this paste at a temperature of 715°C for 45 sec.

In this technique, it is generally difficult to go below 100 micron wide finger lines and this sets the technological limit towards optimization of grid design.

The calculation is based on the following input data : i) Sheet resistivity of Silver : $\rho_{smf} = 3.57 \times 10^{-3} \Omega$

(on the finger lines)

ii) Width of Silver layer = 100µm,

iii) Sheet resistivity of bus bar : $\rho_{smb} = 1.88 \times 10^{-3} \Omega$

(Silver + 80µm solder layer on top)

iv) Specific contact resistance : $\rho_c = 0.37 \times 10^{-3} \Omega.cm^2$ v) Sheet resistivity of silicon n $\stackrel{\circ}{=}$ emitter layer = $\bar{n}_s = 30 \Omega$

vi) Electrical parameter : Jmp= 30 mA/cm⁴

Vmp = 0.48 Volts.

vii) Cell geometry : 10 cm× 10 cm pseudo square.

viii) Finger width : 100 µm

From the calculation with the help of a computer program, We get, Optimized width of Bus bar 2940µm

Optimized finger spacing 2.8 mm

 $p_{cf} = 0.06\%$, $p_{t1} = 1.23\%$, $p_{rf} = 1.09\%$, $p_{rb} = 6.26\%$,

So .Total Electrical loss =Tn = 8.64%

 $P_{sf} = 3.57$, $p_{sb} = 6.25$

So, Total optical loss = Tot = 9.82%

Total power loss = $T_{EL} + T_{OL} = 18.46\%$

It can be observed from the above calculations that the major contribution towards the total loss comes from resistive and shadowing loss of bus bars. This is due to the fact that silver resistivity (screen printed contact) is high so that the larger width of the bus bar has to be taken.

Further, the silver contact has the following disadvantages:

i) Little control on the thickness of the deposited silver.

ii) Expensive material (~ 40% cost of a solar cell comes from the metallization)

iii) Lower resolution of grid pattern.

iv) Considerable wastage of material.

These aforesaid technical problems can be overcome by employing electroless Nickel plating, followed by electroplate copper plating and dip soldering technique.

PLATED METALLIZATION PROCESS :

.

In this technique, a negative screen was printed on the wafer where the diffused mono-silicon wafer was covered with ink except the grid contact lines. The patterned silicon wafers were placed in a Nickel electroless bath [4-5] at 70° C for 20 minutes followed by DI water rinsing several times. The deposited Nickel layer was around 2µm thick. Copper was electrochemically deposited over the Nickel layer by dipping in a copper sulphate solution and constant voltage was supplied with the help of potentiostat arrangement. Around 80µm copper layer was deposited after 30 to 40 minutes of deposition. Then the solder was electrochemically deposited on top of the copper. A thickness of 9-10 microns could be achieved by 30 minutes of deposition.

Using these plated metallizations, the following two types of grid pattern have been considered.

- a) Continuous grid (Fig. 2)
- b) Segmented mesh grid (Fig. 4)

Analysis and Calculation with plated metal grid contacts:

The fractional electrical and optical power losses in each of these proposed grid pattern have been theoretically analyzed and computed numerically using a specially developed computer programme.

The analytical expressions for the continuous grid pattern have already described at the beginning of the model description part. The geometrical parameters for calculation of different losses of segmented mesh grid are shown in fig.3 and actual segmented mesh grid is shown in fig.4.

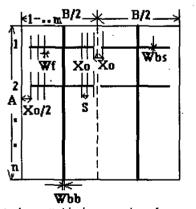


Fig.3 . Different geometrical parameters for segmented mesh grid.

Fig.4 Segmented mesh grid

Now the analytical expressions for segmented mesh grid structure are as follows;

Resistive power losses:

a) Resistive fractional power loss in the emitter layer $p_{ti} = (1/12)p_s s^2 (J_{mp}/V_{mp})c_1$

b) Fractional resistive power loss in fingers $p_{rf} = (1/3)\rho_{smf}(S/W_f)l_b^2(J_{mp}/V_{mp})c_2$

c) Fractional resistive power loss due to contact resistance pd = 0c(S/Wt)(Jmd/Ym)C3, Where pc = Specific

 $p_{cf} = \rho_c(S/W_f)(J_{mp}/V_{mp})c_3$, Where $\rho_c = Specific contact resistance of the metal with the silicon in U.cm².$ d) Fractional resistive power loss in the small bus bars

 $p_{rb1} = (2/3)bl_b^2(\rho_{smb1}/W_{b1})(J_{rm}/V_{mp})C_3$

where \tilde{n}_{smb1} is the sheet resistivity of the small bus bars. e) Fractional resistive power loss in the big bus bars

 $p_{rb2} = (2/3)A^2 l_b (p_{smb2}W_{b2}) (J_{mp}/V_{mp}) c_3$

where \tilde{n}_{smb2} is the sheet resistivity of the big bus bars and I_b = $(B/2-x_o-W_{b2})/2$.

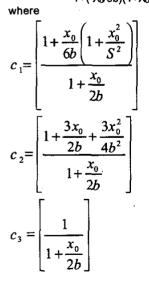
Optical power losses :

a) Fractional optical power loss in the fingers = $p_{sf} = (w \notin S)c_3$

b) Fractional optical power loss in the small bus bars

 $p_{sb1}=(W_{b1}/2b)c_3$ c)Fractional optical power loss in the big bus bars

 $p_{sb2}=(W_{b2}/2l_b)c_3$ 1+(X_0/6b)(1+X_0^2/S^2)



0-7803-7471-1/02/\$17.00 ©2002 IEEE

The following inputs have been used for the numerical calculations:-

- i) Cell geometry= 10cm×10cm square.
- ii) Electrical parameters : Jmp=30mA/cm²
 - V_{mp}=0.48Volt
- iii) Sheet resistance of emitter layer=ps=30 ohms/
- iv) Sheet resistivity of the finger and small bus bars multi layer metals=0.228 mohms/
- v) Sheet resistivity of big bus bar soldered with interconnecting strip = 0.083 mohms/
- vi) Specific contact resistance of the metal layers with silicon = 16.7 mohms/cm²

The calculations have also been done by taking big bus bar width in steps. It can be shown that if $(W_{b2})_{opt}$ is the optimum width for uniform big bus bar, then the starting width of the bus bar in steps will be given by

 $NW_{b2} = \sqrt{3} [W_{b2}]_{opt}$, where N = number of small bars. total loss.

RESULT AND DISCUSSION

The table-1 shows the geometrical dimensions of the grid pattern viz. widths of the finger lines(W_i),small bus bar (W_{bs}), big bus bar(W_{bb}),separation between finger segments (X_o) etc. for optimized minimum

Table-1

Normalized power losses for optimized grid patterns of different types

| Grid pattern | Continuous grid | Segmented mesh grid |
|---|----------------------------------|--|
| Parameters used | S=2.40mm W;=100µm W₀=640µm | S=2.40mm W=100μm Wbs=100μm Wbs=670μm Xo=5mm N=5 |
| Total normalized optical loss(%) | 5.46 | 5.11 |
| Total normalized electrical power loss(%) | 6.10 | 4.93 |
| Total normalized power loss(%) | 11.57 | 10.04 |

It is evident from table-1 that optimized total losses in all the two grid patterns are only marginally different. The selection of the grid pattern is therefore dictated by the technology to be used for grid formation. If standard silver paste screen printing processing is to be used, the continuous grid finger pattern is alright. However, for plating processing, since metal is deposited inside the narrow channels, the possibility of having discontinuities increases with increasing length of the narrow finger lines. This is why a segmented mesh grid pattern is more compatible to plating processes. Further with plating process, the thickness of the grid fingers and bus bars can be increased to the desired value in order to attain lower sheet resistivity of the fingers and bus bars so that narrower fingers could be used for the same specification electrical loss while the optical loss will decrease further with increasing separation between the segments of the grid finger. The sheet resistance of the diffused layer can also be optimized for the separation between the grid segments.

It may be pointed out that the minimum finger width has been taken to be 100 micron. Since it is understood that it may not be possible to realize lower widths with the available screen printing technology. With the improvement of screen printing technology, it is expected that grid finger widths as low as 30-50 micron using plated technology can be realized.

CONCLUSION

The different grid structures based on plated metal contact on silicon solar cells have been analyzed in detail. The segmented mesh grid structure with uniform big bus bar are found to be attractive from the point of view of both technical and theoretical considerations.

ACKNOWLEDGEMENT

The work was carried out jointly by the School of Electrical and Computer Engineering, Sungkyunkwan University south Korea and IC Design and Fabrication Centre ,Department of Electrical and Telecomm. Engineering, Jadavpur University, India. The work was carried out under BK-21 project.

REFERENCES

[1] H.B.Serrze, "Optimizing solar cell performance by simultaneous consideration of grid pattern design and interconnect configuration", Proc. IEEE PVSC, 1978, pp609-613.

[2] S.Khemthong, P.A.Iles, S.Soclof and K.S.Ling " Fabrication experience with high efficiency silicon concentrator cells ", Proc. IEEE PVSC, 1978,pp1046-1051.

[3] M.A.Green , " Solar Cells ", Prentice-Hail, inc., Englewood Cliffs, N.J.07632 , 1982.

[4] U.Gangopadhyay ,K.Shina and H.Saha," Autocatalytic nickel plating on different silicon surfaces", Indian J. Phys. 61A, 1987,pp266-271.

[5] S.Bandopadhyay, U.Gangopadhyay K.Mukhopadhyay, H .Saha," Nickel silicide contact for silicon solar cells",Bull. Mater.Sci. Vol. 15, No. 5, 1992, pp473-479.