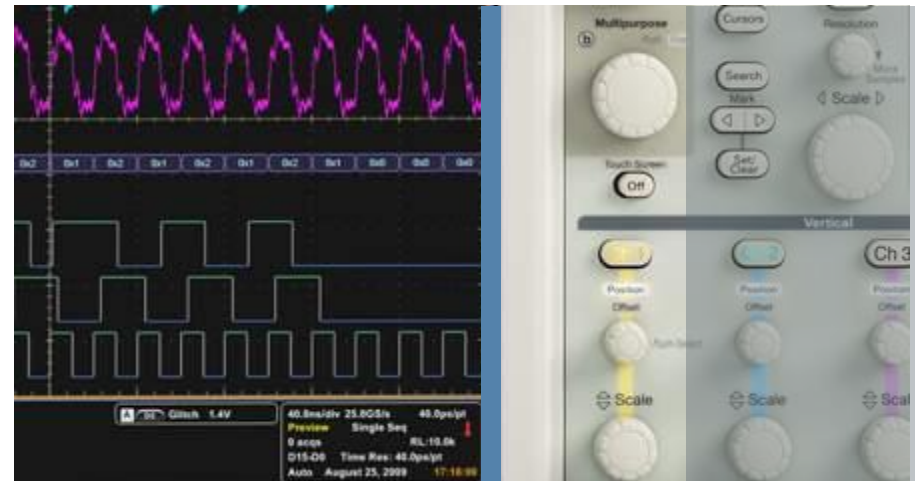
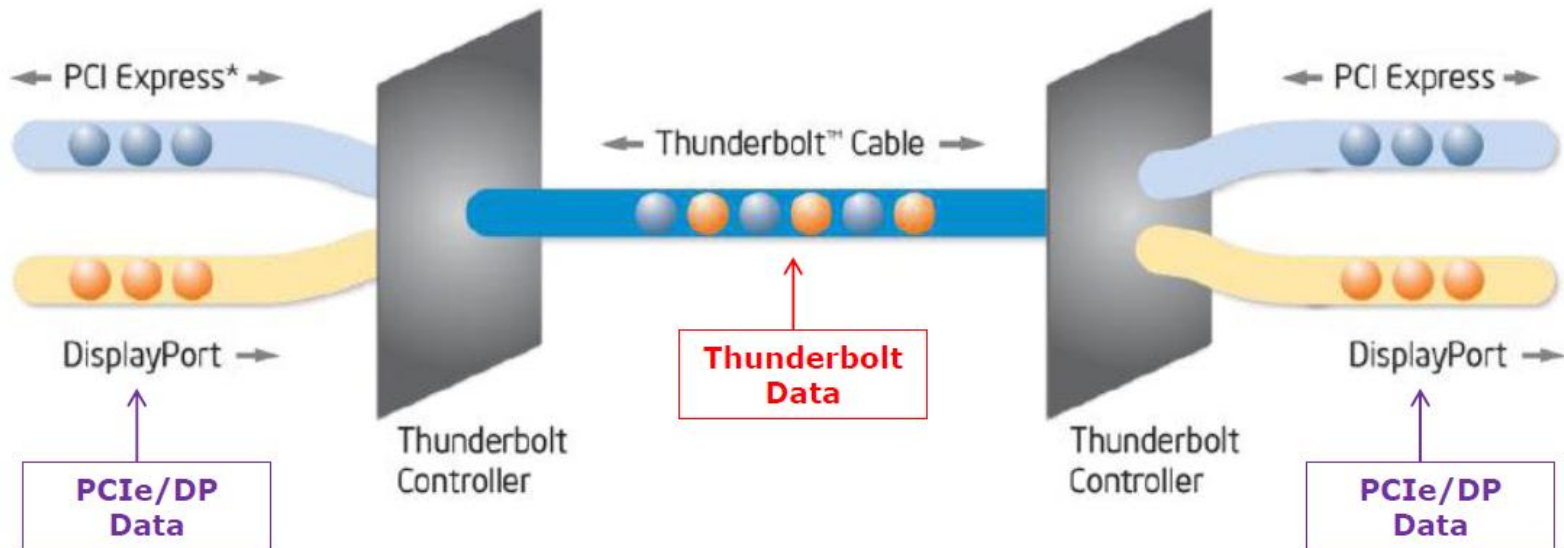


# PHY Validation of Thunderbolt & DisplayPort



# Thunderbolt Overview

- High Speed Data Bus for PC's
  - Brought to market by Intel/Apple in 2011
  - Interoperable with DisplayPort
- Thunderbolt signaling is dual NRZ (64/66b Encoded)
  - 10.3125 Gb/s data rate
  - It utilizes SFP+ technology with 2 diff Tx and Rx pairs.



# Thunderbolt Electrical Validation

Tektronix DPOJET  
Thunderbolt .7 MOI  
Manual Test



Thunderbolt (.7 Spec  
Revision)  
10.3125Gbps

Thunderbolt  
(future Interop)

Display Port DP1.2

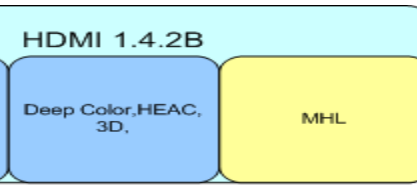
RBR (1.6Gbps),

HBR (2.7Gbps)

HBR2 (5.4Gbps)

DP++

Tektronix DP12  
Full test  
automation



Tektronix HDMI  
HT3/HEAC/MHL  
Full test  
automation



Tektronix SATA  
TSG/SATA-RSG  
Full test  
automation



# Dual Port Device Compliance Test Summary

## ■ Physical Layer Testing

– (Rev 0.7 Spec)

1. TBT Transmitter MOI
2. TBT Receiver MOI
3. TBT Return Loss MOI
4. DP Source MOI
5. DP++ (HDMI) Source MOI
6. Power Delivery MOI

## ■ Functional Testing

– Thunderbolt Functional CTS  
Rev 3.0.1

1. ROM Validation
2. Basic Device Functionality
3. EFI
4. Downstream Device Functionality
5. Downstream Display Functionality
6. Extended Test Functionality
7. Complex Topology
8. DUT Specific Verification
9. Negative Testing
10. Firmware Update Validation

CTS – Compliance Test Specification

MOI – Method of Implementation (Test Procedure)

# Single Port Device Compliance Test Summary

## ■ Physical Layer Testing

– (Rev 0.7 Spec)

1. TBT Transmitter MOI
2. TBT Receiver MOI
3. TBT Return Loss MOI
4. Power Consumption

## ■ Functional Testing

– Thunderbolt Functional CTS  
Rev 2.4 (IBL 488434)

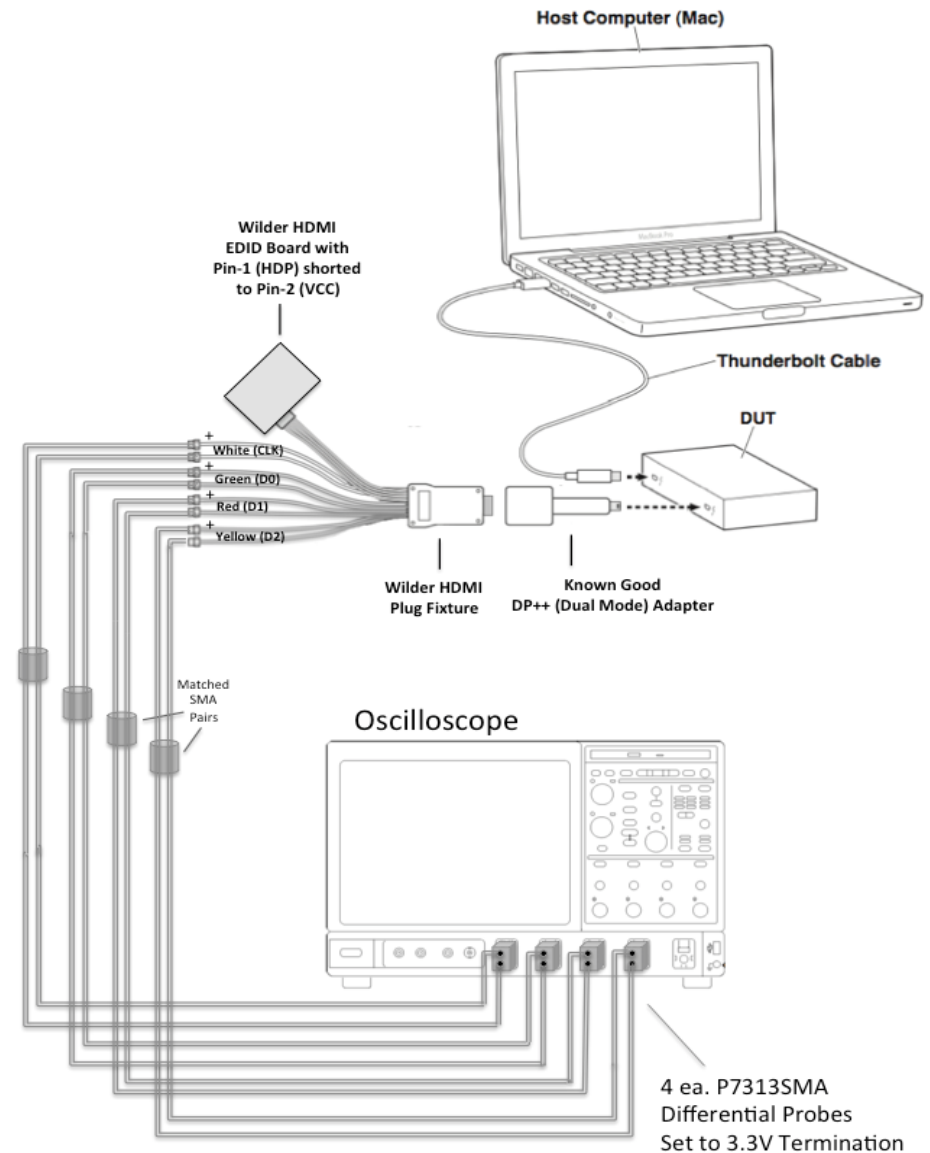
1. ROM Validation
2. Basic Device Functionality
3. EFI
4. DUT Specific Verification
5. Negative Testing
6. Firmware Update Validation

CTS – Compliance Test Specification

MOI – Method of Implementation (Test Procedure)

# HDMI Test Setup

- DSA70804C or higher
- SMA Differential Probes
  - Provides 3.3V bias
- HT3 HDMI Compliance SW
- Mac or equivalent tool used to control downstream port on a 2 port device
- Both ports tested

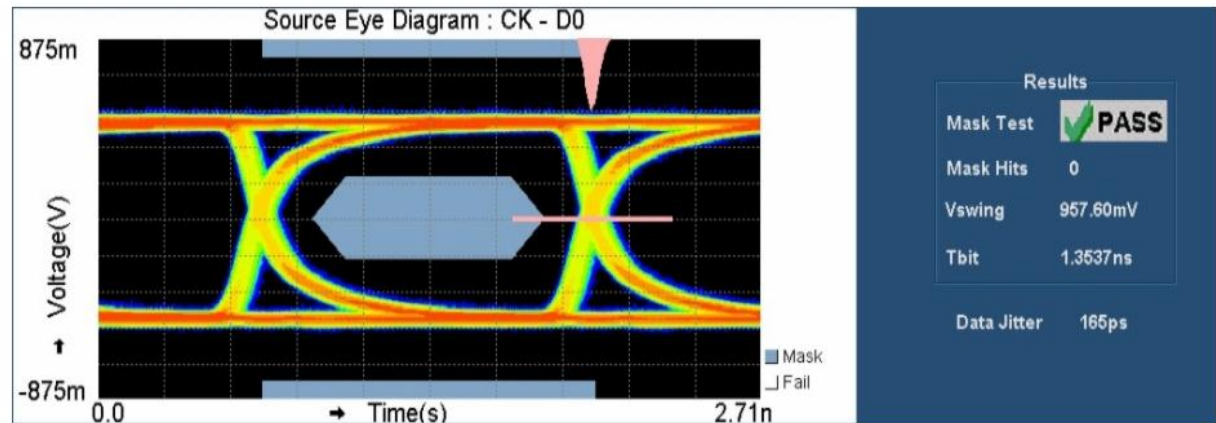


# Example of HDMI Passing Results

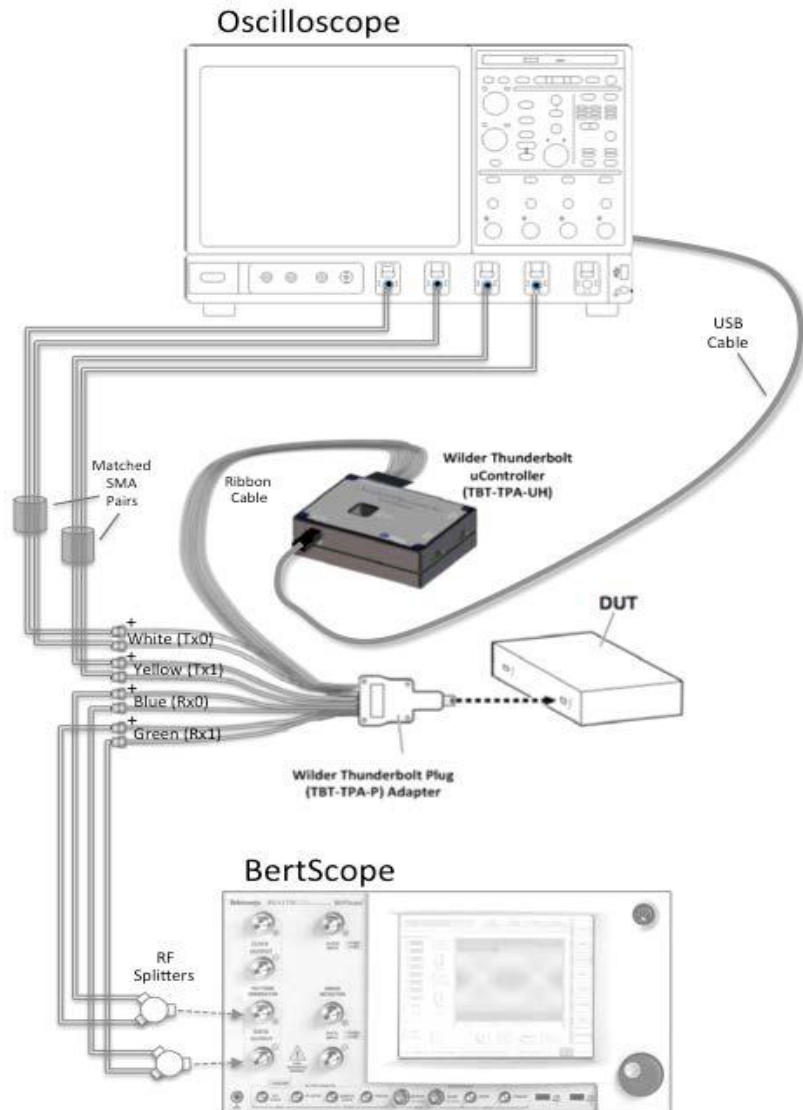
## Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	<a href="#">7-9 : Source Clock Jitter</a>	CK	Clock Jitter < 0.25*Tbit;	0.08*Tbit	Pass
2	<a href="#">7-10 : Source Eye Diagram</a>	CK - D0	Data Jitter < 0.3*Tbit;	0.12*Tbit	Pass
3	<a href="#">7-10 : Source Eye Diagram</a>	CK - D1	Data Jitter < 0.3*Tbit;	0.12*Tbit	Pass
4	<a href="#">7-10 : Source Eye Diagram</a>	CK - D2	Data Jitter < 0.3*Tbit;	0.1*Tbit	Pass
5	<a href="#">7-6 : Source Inter-Pair Skew</a>	D0 - D1	Skew < 0.2*TPixel;	0.007*TPixel	Pass
6	<a href="#">7-6 : Source Inter-Pair Skew</a>	D1 - D2	Skew < 0.2*TPixel;	0.012*TPixel	Pass
7	<a href="#">7-6 : Source Inter-Pair Skew</a>	D2 - D0	Skew < 0.2*TPixel;	0.005*TPixel	Pass
8	<a href="#">7-4 : Source Rise Time</a>	CK	75.00ps < TRISE;	220.23ps	Pass
9	<a href="#">7-4 : Source Rise Time</a>	D0	75.00ps < TRISE;	208.34ps	Pass
10	<a href="#">7-4 : Source Rise Time</a>	D1	75.00ps < TRISE;	210.28ps	Pass
11	<a href="#">7-4 : Source Rise Time</a>	D2	75.00ps < TRISE;	223.47ps	Pass
12	<a href="#">7-4 : Source Fall Time</a>	CK	75.00ps < TFALL;	212.71ps	Pass
13	<a href="#">7-4 : Source Fall Time</a>	D0	75.00ps < TFALL;	219.38ps	Pass
14	<a href="#">7-4 : Source Fall Time</a>	D1	75.00ps < TFALL;	208.07ps	Pass
15	<a href="#">7-4 : Source Fall Time</a>	D2	75.00ps < TFALL;	254.07ps	Pass
16	<a href="#">7-8 : Max Duty Cycle</a>	CK	--	--	Error
17	<a href="#">7-8 : Min Duty Cycle</a>	CK	--	--	Error

## Waveform/Plot



# Automated Thunderbolt Tx Testing



## Recommended Equipment

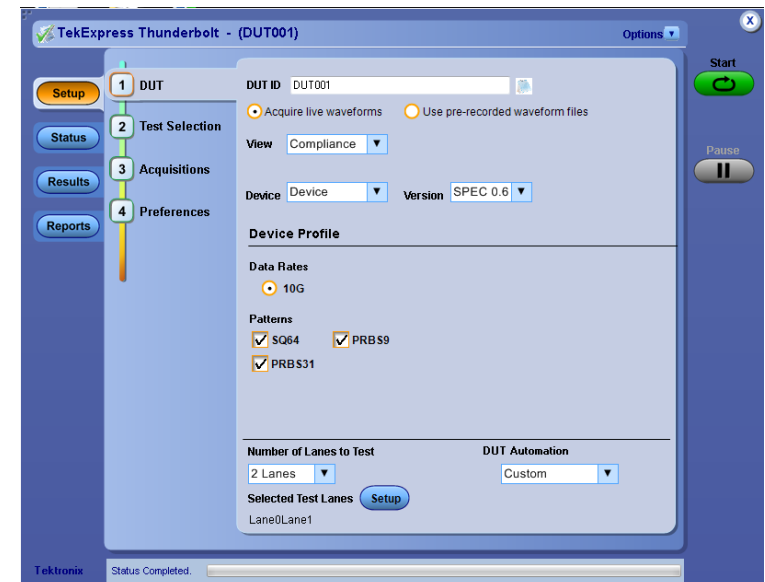
- DPO/DSA/MSO71604 ( $\geq 16$  GHz BW)
- BSA125C (crosstalk source)
- Option DJA (DPOJET)
- Option TBT-TX (TekExpress)
- TF-TB-TPA-P (Plug fixture) & TBT-TPA-UH (port microcontroller)



# Option TBT-TX

## Compliance Automation Software

- Automates scope setup & compliance measurements per the Tek Thunderbolt MOI
- Fast test execution
  - Simultaneous two lane testing
  - Automated DUT state control for devices
- User-selectable tests
- Creates complete test report



# Thunderbolt Transmitter Testing

- **Step 1: Select Measurement Setup**

The screenshot displays the TekExpress Thunderbolt software interface. The window title is "TekExpress Thunderbolt - (Untitled)\*". On the left, a vertical navigation pane shows four steps: 1. DUT (highlighted in orange), 2. Test Selection, 3. Acquisitions, and 4. Preferences. Below the navigation pane are buttons for "Setup", "Status", "Results", and "Reports". The main area is titled "DUT" and contains the following configuration options:

- DUT ID: DUT001
- Acquire live waveforms (selected) / Use pre-recorded waveform files
- View: Compliance
- Device: Device / Version: SPEC 0.7
- Device Profile section with checked patterns: SQ32, PRBS11, and PRBS31.
- Number of Lanes to Test: 2 Lanes
- DUT Automation: Manual
- Selected Test Lanes: Lane0Lane1 (with a "Setup" button next to it)

On the right side of the interface, there are "Start" and "Pause" buttons. The "Start" button is green with a circular arrow icon, and the "Pause" button is grey with a vertical bar icon. At the bottom left, the Tektronix logo is visible, and the status bar shows "Status Ready".

# Thunderbolt Transmitter Testing

- Step 2: Select Measurements (total 18 measurements)

The screenshot displays the TekExpress Thunderbolt software interface. The title bar reads "TekExpress Thunderbolt - (Untitled)\*" with an "Options" dropdown and a close button. On the left, a vertical navigation bar shows four steps: "1 DUT" (checked), "2 Test Selection" (highlighted), "3 Acquisitions", and "4 Preferences". Below this are buttons for "Setup", "Status", "Results", and "Reports". The main area features a list of 15 measurements under the "Thunderbolt Tx" category, all of which are checked. Above the list are "Deselect All", "Select Required", and "Select All" buttons. Below the list is a "Test Description" field and "Schematic" and "Configure" buttons. On the right side, there are "Start" and "Pause" buttons. The bottom status bar shows "Tektronix" and "Status Ready".

Options

Start

Pause

Setup

Status

Results

Reports

1 DUT

2 Test Selection

3 Acquisitions

4 Preferences

Deselect All

Select Required

Select All

Thunderbolt Tx

- PHY 1.1\_Unit Interval (min) measurement
- PHY 1.2\_SSC Spread Deviation
- PHY 1.3\_SSC Modulation Frequency measurement
- PHY 1.4\_SSC Phase Deviation
- PHY 1.5\_SSC Phase Slew Rate
- PHY 1.6\_Total Jitter (TJ1) measurement
- PHY 1.7\_Total Jitter (TJ2) measurement
- PHY 1.8\_Total Jitter (TJLF) Low Frequency measurement
- PHY 1.9\_Eye Width measurement
- PHY 1.10\_Eye Height measurement
- PHY 1.11\_Mask Hits measurement
- PHY 1.12\_Rise Time measurement
- PHY 1.13\_Fall Time measurement
- PHY 1.14\_AC common mode voltage Peak to Peak
- PHY 1.15\_Data Dependent Jitter measurement

Test Description

Schematic

Configure

Tektronix

Status Ready

# Thunderbolt Transmitter Testing

## Step 3: Configure Acquisitions

The screenshot displays the TekExpress Thunderbolt software interface. The left sidebar contains navigation buttons: Setup, Status, Results, and Reports. A vertical progress indicator shows four steps: 1. DUT (checked), 2. Test Selection (checked), 3. Acquisitions (highlighted with a red circle), and 4. Preferences. The main workspace is titled 'TekExpress Thunderbolt - (Untitled)\*' and features an 'Options' dropdown. A 'View Probes' button is located in the top right. Below it, a table lists lane configurations:

Lane	Source	Lane	Source
Lane0+	CH1	Lane1+	CH3
Lane0-	CH2	Lane1-	CH4

Below the table is a 'View Probes' button. The main area contains a list of test names and their corresponding acquisition configurations:

Test Name	Acquisition
PHY 1.15_Data Dependent Jitter measu	Lane0 : PRBS11
PHY 1.16_UJ RJ measurement	
PHY 1.15_Data Dependent Jitter measu	Lane1 : PRBS11
PHY 1.16_UJ RJ measurement	
PHY 1.10_Eye Height measurement	
PHY 1.11_Mask Hits measurement	
PHY 1.4_SSC Phase Deviation	Lane0 : PRBS31
PHY 1.5_SSC Phase Slow Rate	
PHY 1.0_Eye Width measurement	

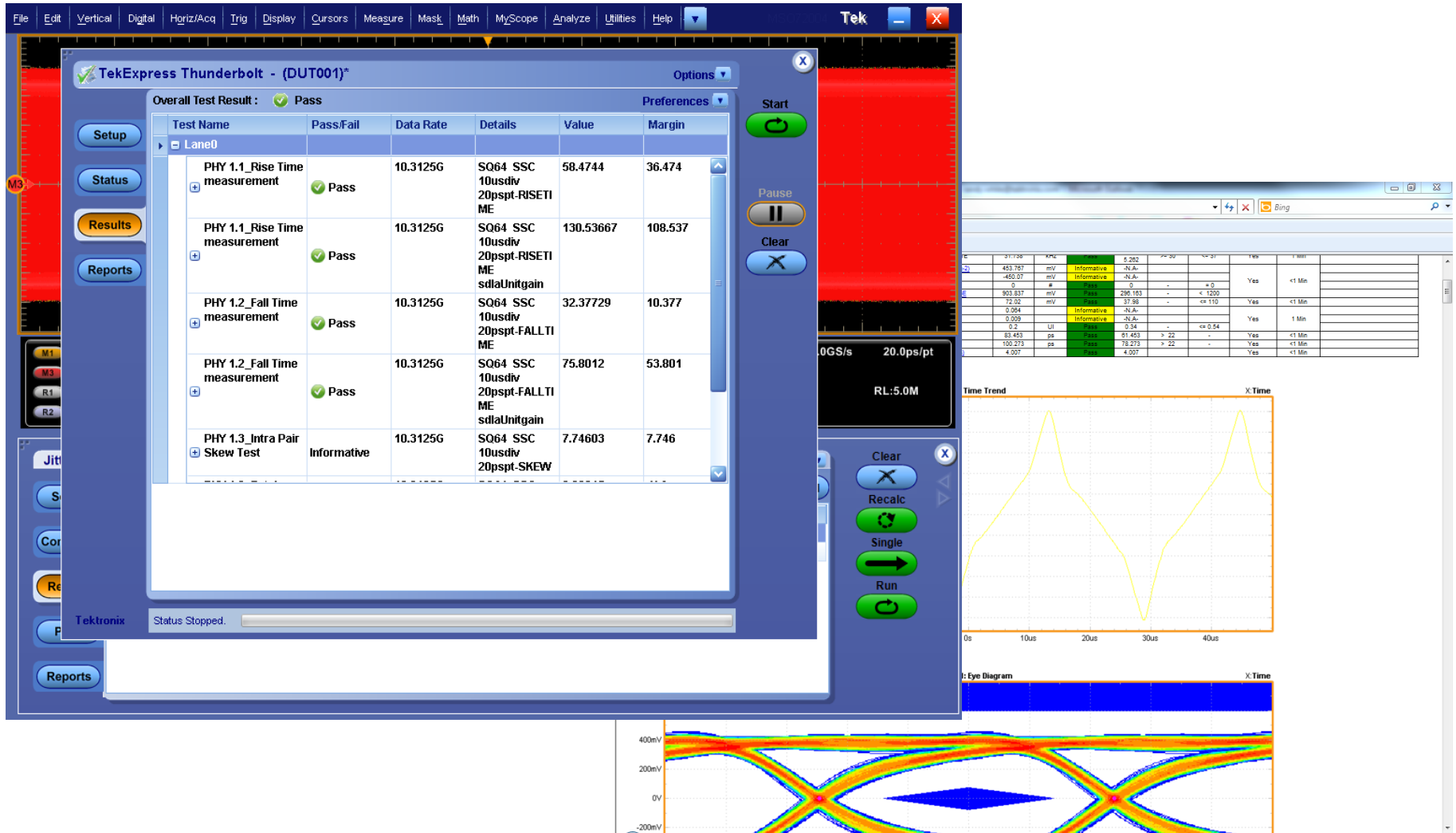
Below the list are 'Acquisition and Save Options':

- Save All Waveforms Before Analysis
- Analyze Immediately - No Waveforms Saved
- Save and Analyze Acquisition In Sequence
- Show Acquire Parameters
- Acquire Step By Step

The 'Signal Validation' dropdown is set to 'Use signal as is - Do...'. The bottom status bar shows 'Tektronix Status Ready'.

# Thunderbolt Transmitter Testing

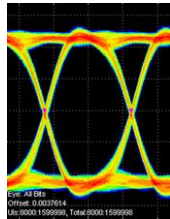
## Step 4: Start Tests and Generate Report



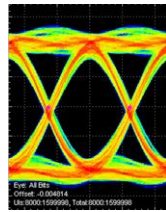
# Test Challenge: De-Embedding

## Transmitter Compliance Testing

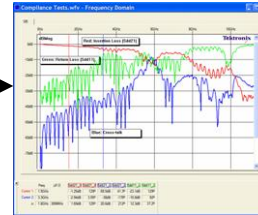
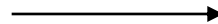
- Host/device compliance point at TP1 (mated plug/receptacle)
- De-embedding required to remove fixture effects
- S-Parameters are acquired from calibration fixture



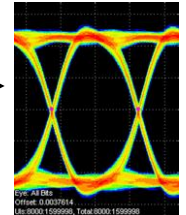
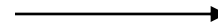
Signal at TP1



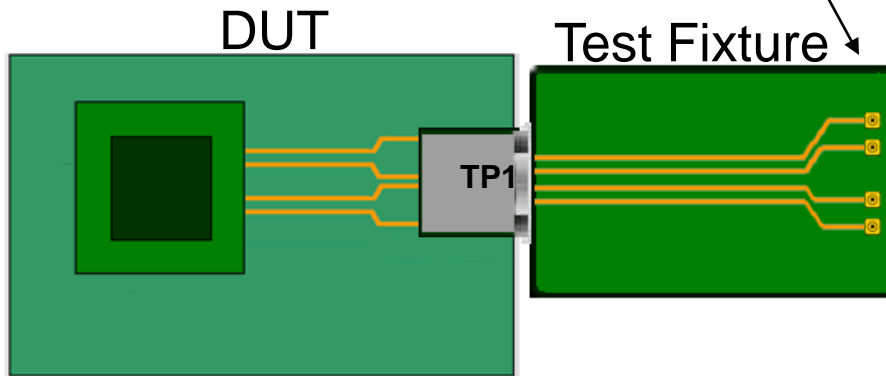
Measured Signal



Apply Sparameters



Signal with Fixture Effects Removed



# Thunderbolt Fixture De-Embed results

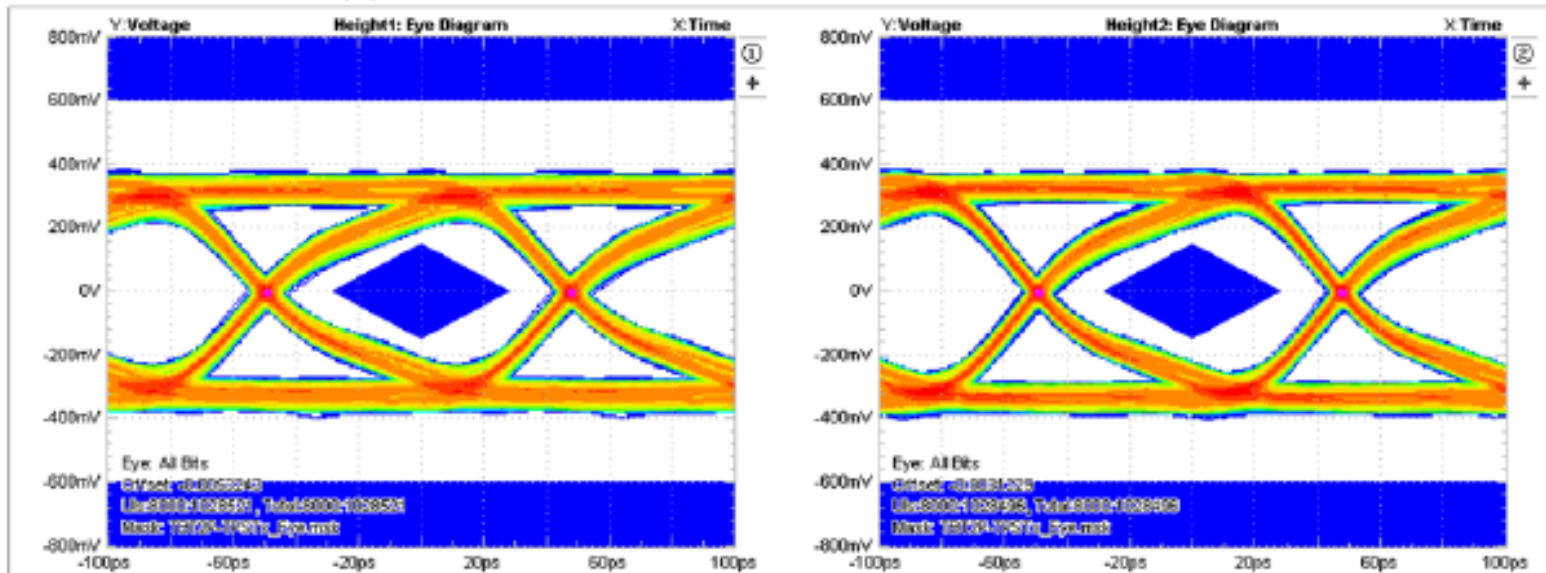
## Measurement Results

Description	Mean	Std Dev	Max	Min	p-p	Population	Max-cc	Min-cc
Height1, Math1	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	370.29mV	0.0000V	370.29mV	370.29mV	0.0000V	1	0.0000V	0.0000V
Height2, Math3	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
Current Acquisition	405.59mV	0.0000V	405.59mV	405.59mV	0.0000V	1	0.0000V	0.0000V
TJ@BER1, Math1	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	19.175ps	0.0000s	19.175ps	19.175ps	0.0000s	1	0.0000s	0.0000s
TJ@BER2, Math3	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s
Current Acquisition	17.304ps	0.0000s	17.304ps	17.304ps	0.0000s	1	0.0000s	0.0000s

Pass/Fail Summary No pass/fail limits are currently selected.

## Plot Images

### Measurement Plot(s)



# Test Challenge: Crosstalk

## Measuring Bounded Uncorrelated Jitter (BUJ) is Critical

- Interconnect and board layout technology is advancing and the greatest area of focus is in reducing the insertion loss and Signal-to-Crosstalk ratio.
- The implications of complex channel interaction can be observed and identified by examining the type and amount of BUJ.
- There is a strong Cause-and-Effect relationship between Crosstalk and BUJ which often gets classified as Random if special steps are not observed.

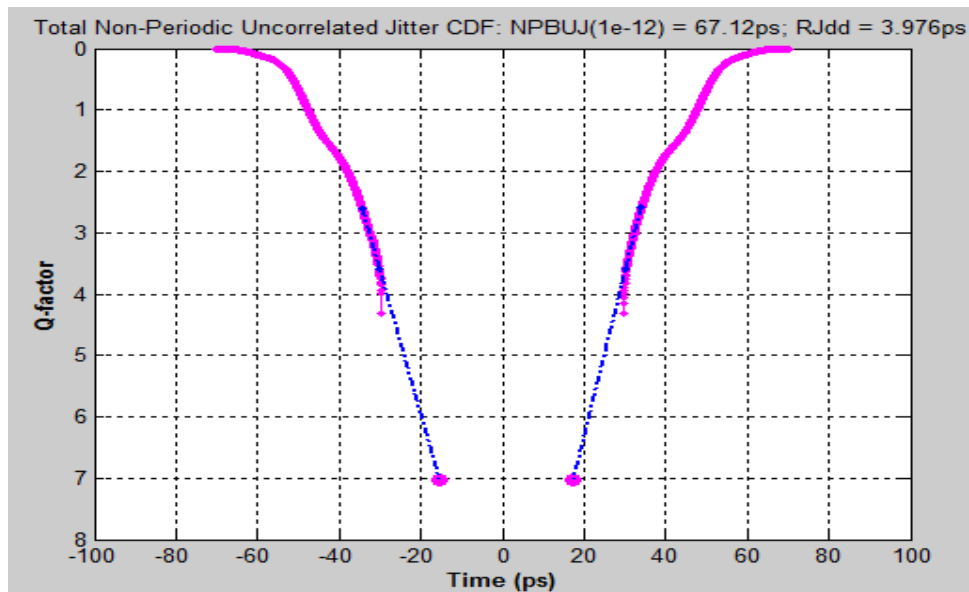
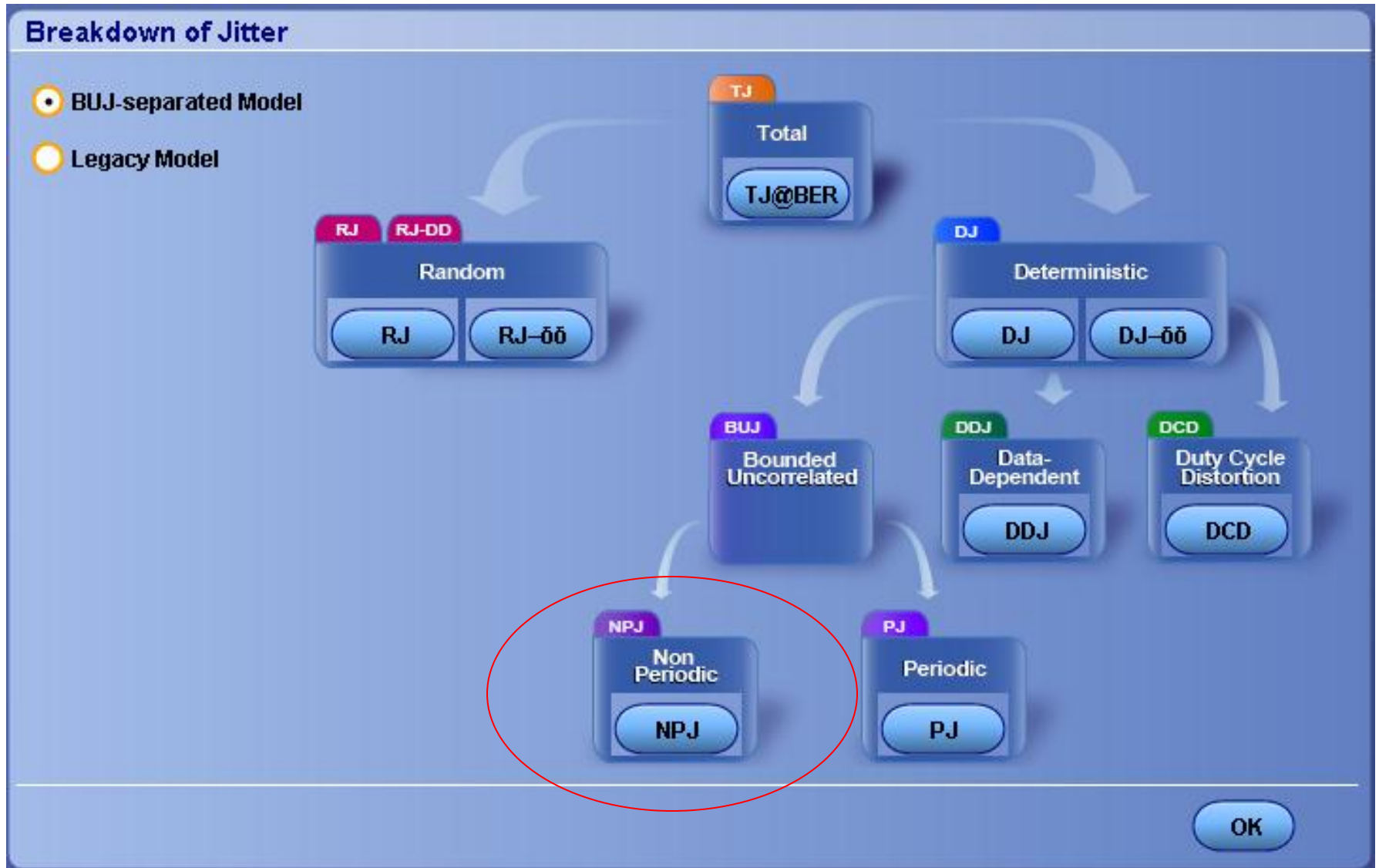


Table 4-6. Stressed Receiver Conditions

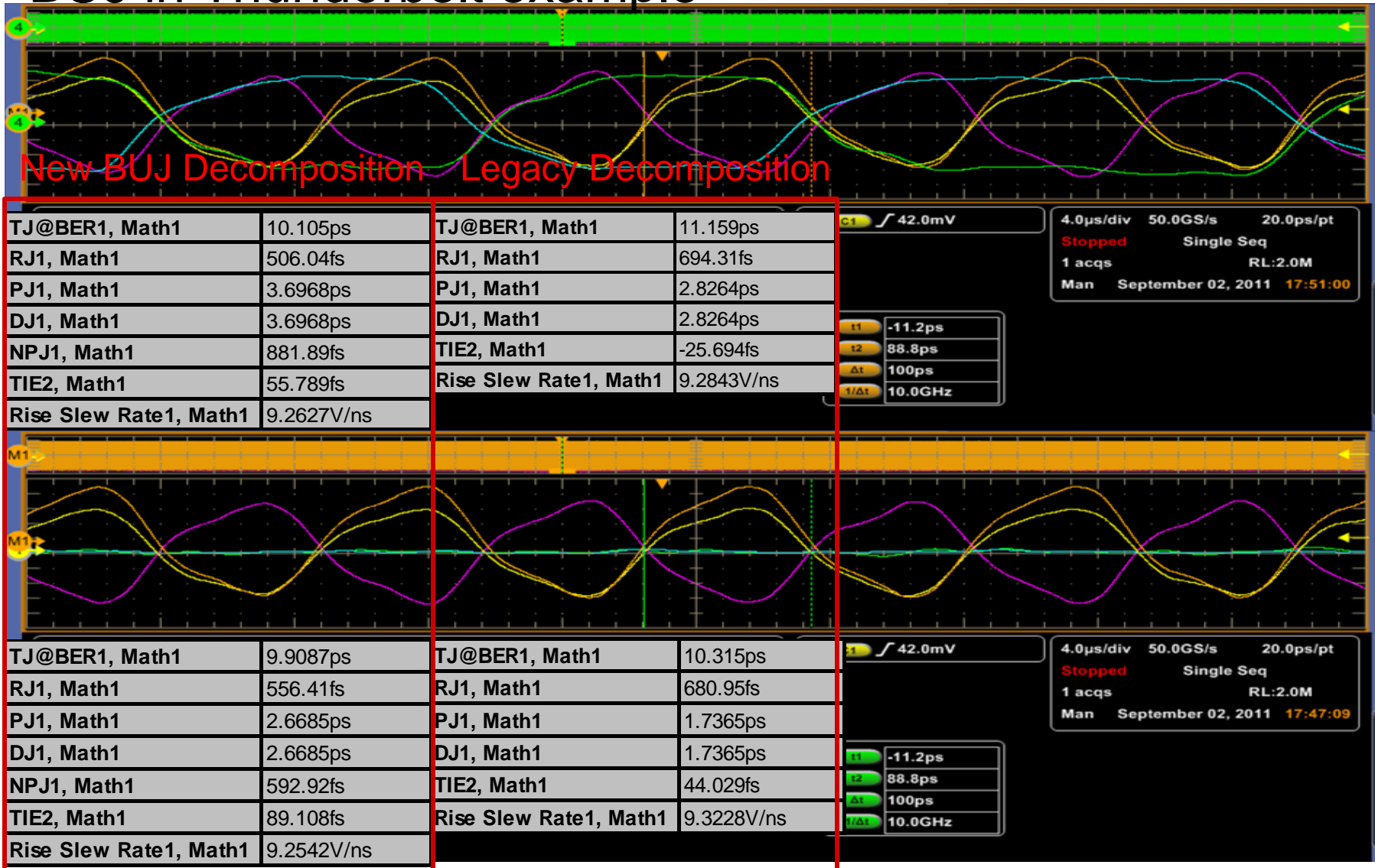
Symbol	Description
Input swing	Inner eye voltage
AC-CM_rms	AC Common Mode Voltage rms
AC-CM_pk_pk	AC Common Mode Voltage pp
<b>BUJ</b>	Bounded Uncorrelated Jitter
DDJ	Data Dependent Jitter
RJ	Random Jitter
TJ	Total Jitter



# BUJ in real time jitter analysis




# BUJ in Thunderbolt example



# Receiver Testing Overview

- MOI critical to Rx Test
- Includes step-by-step procedure along with setup files for calibration





Tektronix GRL Confidential

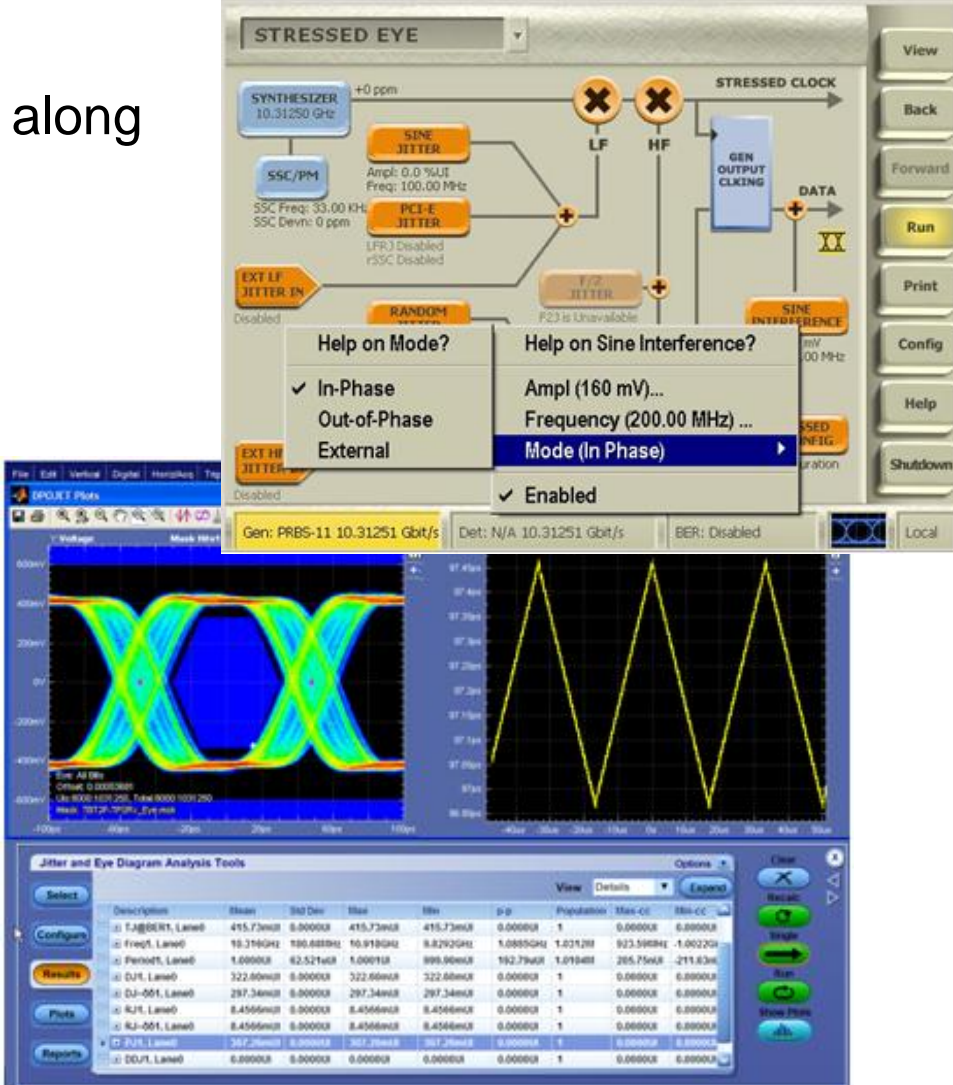
**Thunderbolt™ Device Compliance Test  
 Method of Implementation (MOI)  
 Using Tektronix DSA70000 Series  
 (16 GHz and above)  
 Real Time Oscilloscope and  
 BSA125C BERTScope**

Revision 0.62

(Note: MOI Revision x.x tracks Revision of TBT Interconnect Specification.  
 The second decimal x.xx is reserved for official revisions of the MOI)

Page 1 of 93

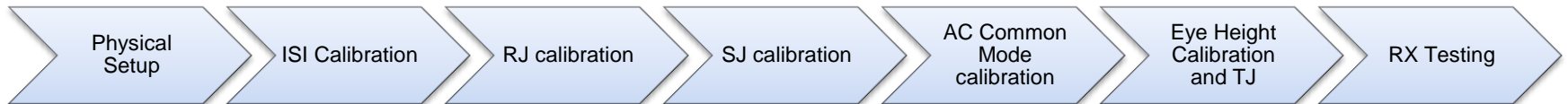
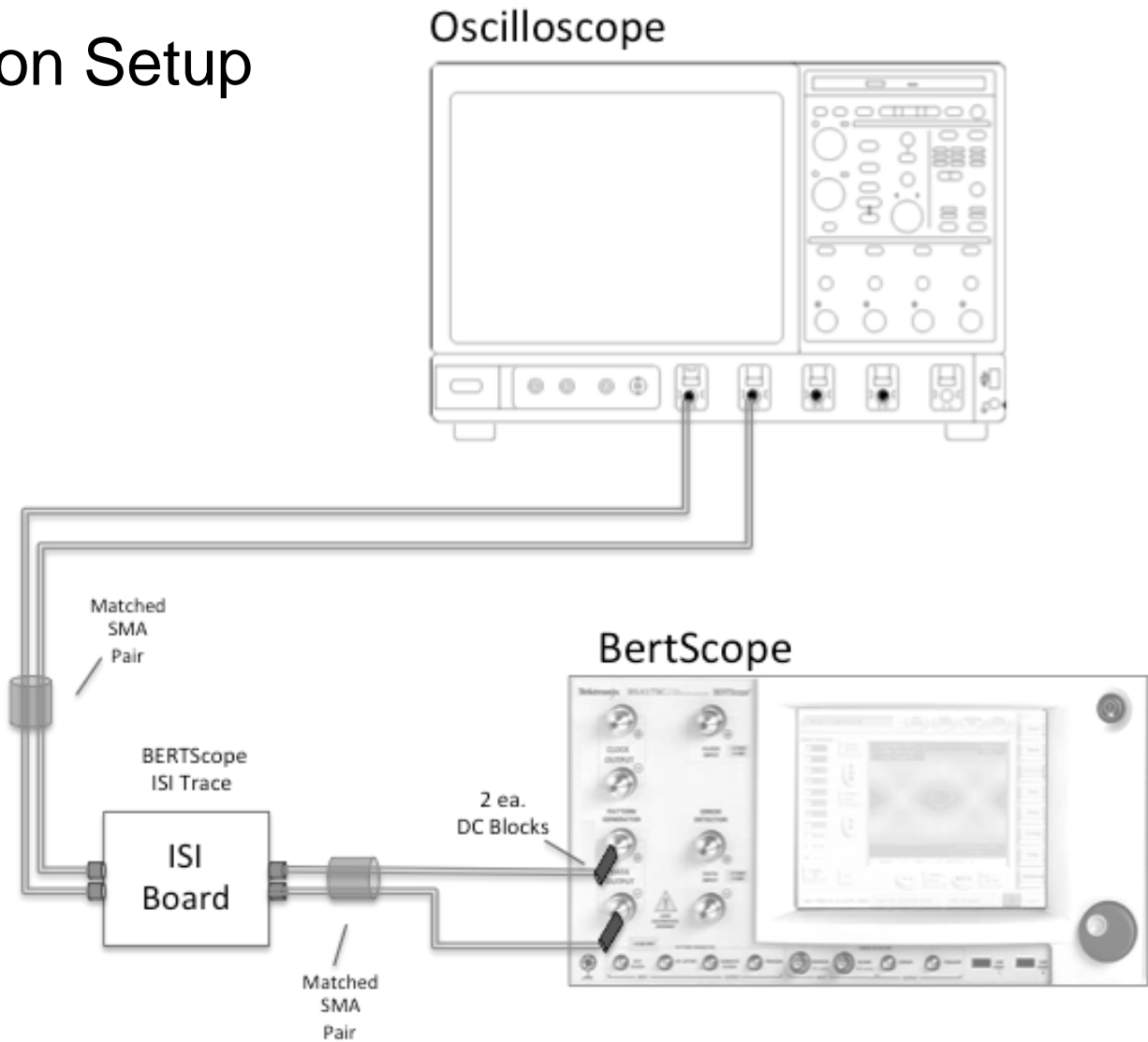


The screenshot displays the 'STRESSED EYE' software interface. The top part shows a block diagram of a signal path starting with a 'SYNTHESIZER' (10.31250 GHz) and 'SSC/PM' block. The signal passes through 'SINE JITTER' and 'PCI-E JITTER' blocks, which are summed together. This is followed by 'EXT LF JITTER IN' and 'RANDOM JITTER' blocks. The signal then goes through 'LF' and 'HF' filters, and a 'GEN OUTPUT CLKING' block. The final output is 'DATA'. A 'SINE INTERFERENCE' block is also present, which is currently set to 'Mode (In Phase)'. The 'SINE INTERFERENCE' block has a 'Help on Sine Interference?' dialog box open, showing options for 'Ampl (160 mV)...', 'Frequency (200.00 MHz) ...', and 'Mode (In Phase)'. The 'Mode (In Phase)' option is selected and highlighted.

The bottom part of the screenshot shows the 'Jitter and Eye Diagram Analysis Tools' table. The table has columns for Description, Mean, Std Dev, Min, Max, p-p, Population, Max CC, and Min CC. The table lists various jitter components and their values.

Description	Mean	Std Dev	Min	Max	p-p	Population	Max CC	Min CC
FJ@BERT, Lane0	415.73ns	0.0000s	415.73ns	415.73ns	0.0000s	1	0.0000s	0.0000s
FreqT, Lane0	10.316GHz	100.688ns	10.919GHz	8.8292GHz	1.0885GHz	1,021,281	923.59MHz	-1.0022GHz
PeriodT, Lane0	1.0000ns	82.521ns	1.0001ns	898.96ns	192.79ns	1,019,481	285.75ns	-211.63ns
DJ1, Lane0	322.60ns	0.0000ns	322.60ns	322.60ns	0.0000ns	1	0.0000ns	0.0000ns
DJ-001, Lane0	297.34ns	0.0000ns	297.34ns	297.34ns	0.0000ns	1	0.0000ns	0.0000ns
RJ1, Lane0	8.4566ns	0.0000ns	8.4566ns	8.4566ns	0.0000ns	1	0.0000ns	0.0000ns
RJ-001, Lane0	8.4566ns	0.0000ns	8.4566ns	8.4566ns	0.0000ns	1	0.0000ns	0.0000ns
PJ1, Lane0	307.28ns	0.0000ns	307.28ns	307.28ns	0.0000ns	1	0.0000ns	0.0000ns
DJTL, Lane0	0.0000ns	0.0000ns	0.0000ns	0.0000ns	0.0000ns	1	0.0000ns	0.0000ns

# Calibration Setup

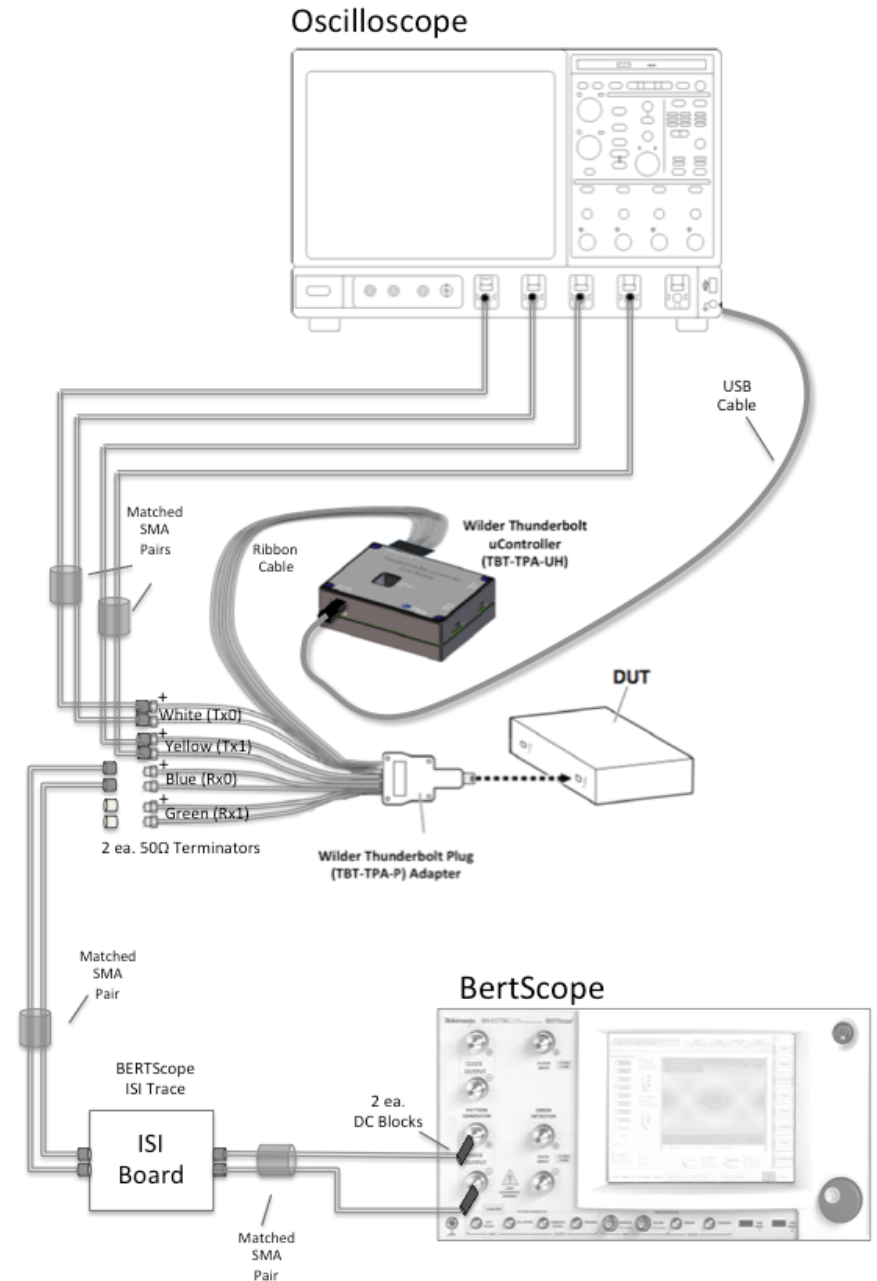


# Rx Testing

## Steps to Run BER test:

- Attach DUT & microcontroller
- Turn on required stresses
- Run RX BER script for 6 mins

```
C:\Program Files\Intel Corpora
Rev 1.1
DUT found is LR
Please wait for Lane check
Lane under test is Lane 0
Wait for BER testing
BER is 0.000000e+000
Symbol_count is 2110019967936
Error_count is 0
Please hit Enter to close the window
=
```



# Complete Thunderbolt Instrument Portfolio

## Receiver Tests/Active Cable Tests

Receiver silicon and system margin testing.

Tj, Rj, DDJ, BUJ, AC-CM

**BSA125C** 12.5 Gb/s BERTScope

**DPP125B** Digital Pre-Emphasis Preprocessor

**CR125A** Clock Recovery Unit

**TF-TB-TPA-P/R** Plug & Receptacle Test Fixtures



## Channel Tests

Return Loss (HF,LF)  
(SDD11,SDD22)

Common Mode Return Loss  
(SCC22)

Channel Insertion Loss (SDD21)

Near End Crosstalk (NEXT)

**DSA8300** Sampling Oscilloscope

**80E04** 20 GHz TDR Sampling Module

**80SICON** S-Parameter Analysis Software for DSA8300

**TF-TB-TPA-P** Test Fixture



## Transmitter Tests

AC Parametric measurements

Jitter

Eye Opening

**DSA71604C** with option **TBT-TX**

**DPOJET** Jitter Analysis software

**TF-TB-TPA-P** Test Fixture



# Debug Example

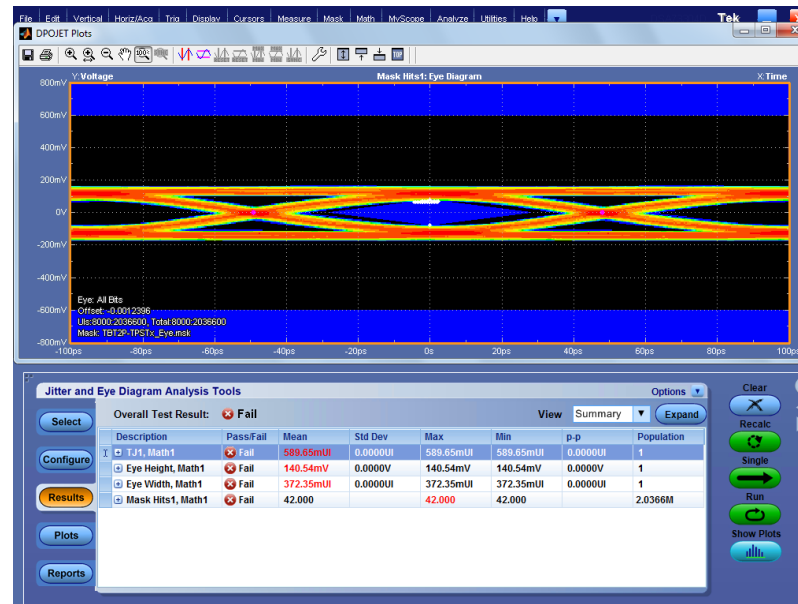
- TBT design fails during certification
  - Report shows voltage/timing failures
- What's the next step?



Test Name	Lane	Pattern	Speed	SSC	Measurement Details	Measured value	Units	Test Result
PHY 1.5_Eye Height measurement	Lane0	PRBS31	10.3125G	SSC	HEIGHT	147.238	mV	Fail
PHY 1.6_Eye Width measurement	Lane0	PRBS31	10.3125G	SSC	WIDTH	0.404	UI	Fail
PHY 1.9_Unit Interval (min) Measurement	Lane0	PRBS31	10.3125G	SSC	<a href="#">PERIOD(Fig-1)</a>	97.225	ps	Pass
PHY 1.10_SSC Modulation Frequency Measurement	Lane0	PRBS31	10.3125G	SSC	SSCMODRATE	31.76	kHz	Pass
PHY 1.7_Max Differential Voltage Measurement	Lane0	PRBS31	10.3125G	SSC	<a href="#">EYEHIGH(Fig-2)</a>	484.697	mV	Informative
	Lane0	PRBS31	10.3125G	SSC	<a href="#">EYELOW</a>	-480.843	mV	Informative
	Lane0	PRBS31	10.3125G	SSC	<a href="#">MASKHITS</a>	154	#	Fail
	Lane0	PRBS31	10.3125G	SSC	<a href="#">MAXDIFFVGE</a>	965.54	mV	Pass
PHY 1.4_AC common mode voltage Peak to Peak	Lane0	PRBS9	10.3125G	SSC	PK2PK	58.355	mV	Pass
PHY 1.8_Total Jitter measurement	Lane0	PRBS31	10.3125G	SSC	DJ	0.127		Informative
	Lane0	SQ64	10.3125G	SSC	RJ	0.006		Informative
	Lane0	SQ64	10.3125G	SSC	TJBER	0.56	UI	Fail
PHY 1.1_Rise Time measurement	Lane0	SQ64	10.3125G	SSC	RISETIME	83.023	ps	Pass
PHY 1.2_Fall Time measurement	Lane0	SQ64	10.3125G	SSC	FALLTIME	104.417	ps	Pass
PHY 1.3_Intra Pair Skew Test	Lane0	SQ64	10.3125G	SSC	<a href="#">SKEW(Fig-3)</a>	4.231		Pass

# Drilling into Root Cause

- Import saved waveforms into DPOJET
- Re-run measurements that fail
- Based on results can:
  - Compare against addition plots
  - Modify DPOJET or acquisition settings (filters, RL, etc.)
  - Investigate signal anomalies with DPOJET sync features

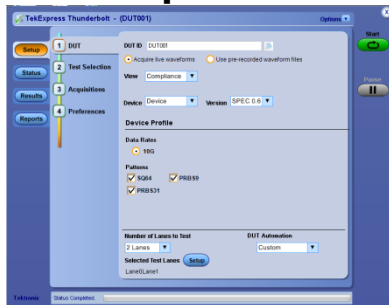




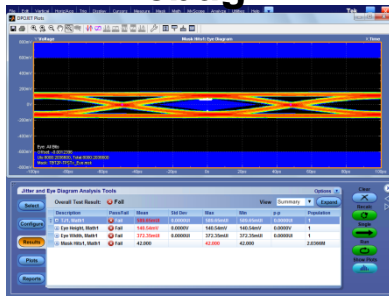
# Final Resolution

- Voltage droop on D- (Ch3) causes amplitude imbalance
- Customer suspects RC time constant not set correctly (DC block/pull down)

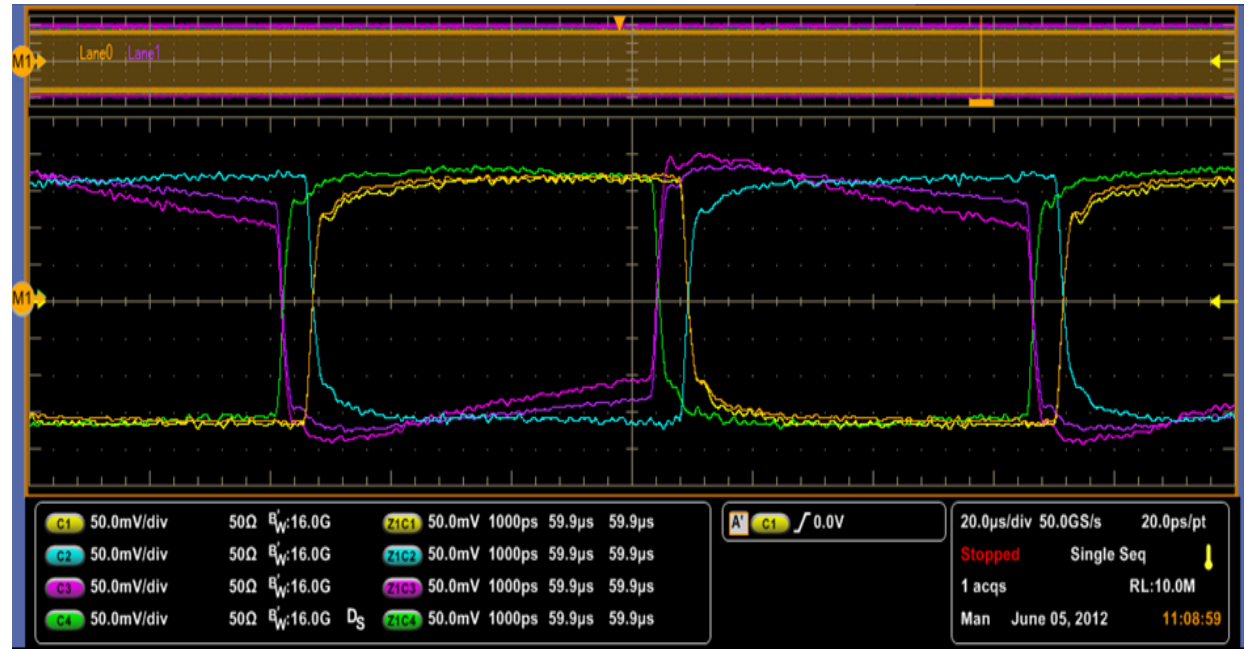
## Compliance



## Debug



## Root Cause



# DEMO



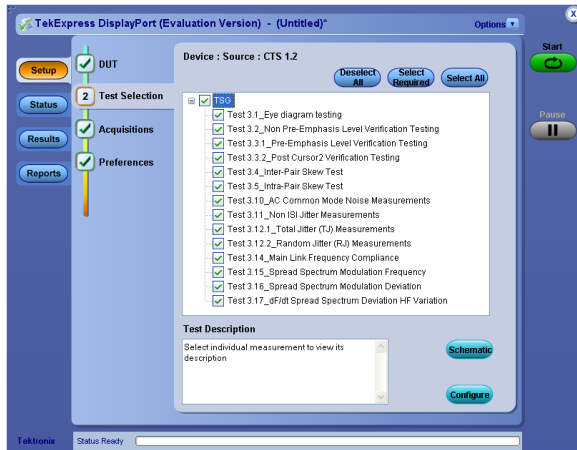
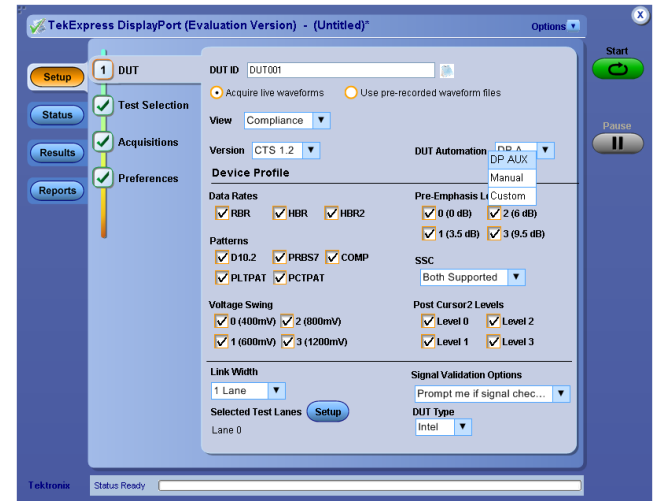
# Display Port Source testing

1. Select

2. Acquire

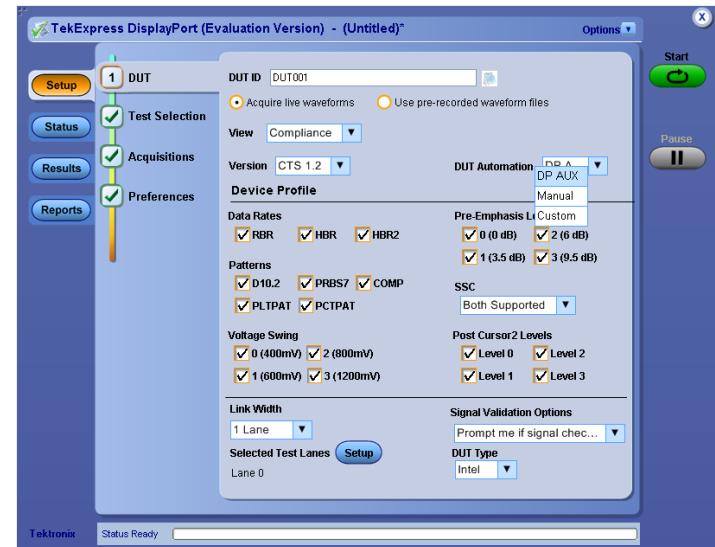
3. Analyze

Can it be just that easy?



# Customer needs in Display Port testing

- Challenges
  - Device State control
  - Measurements algorithms
  - Setups
- Requirements
  - Straight forward operations and setups
  - Complete testing for both single ended and differential measurements
  - Flexibility in testing
- Results
  - Pass or Fail
  - Margins and Limits
  - Complete and easy to read report



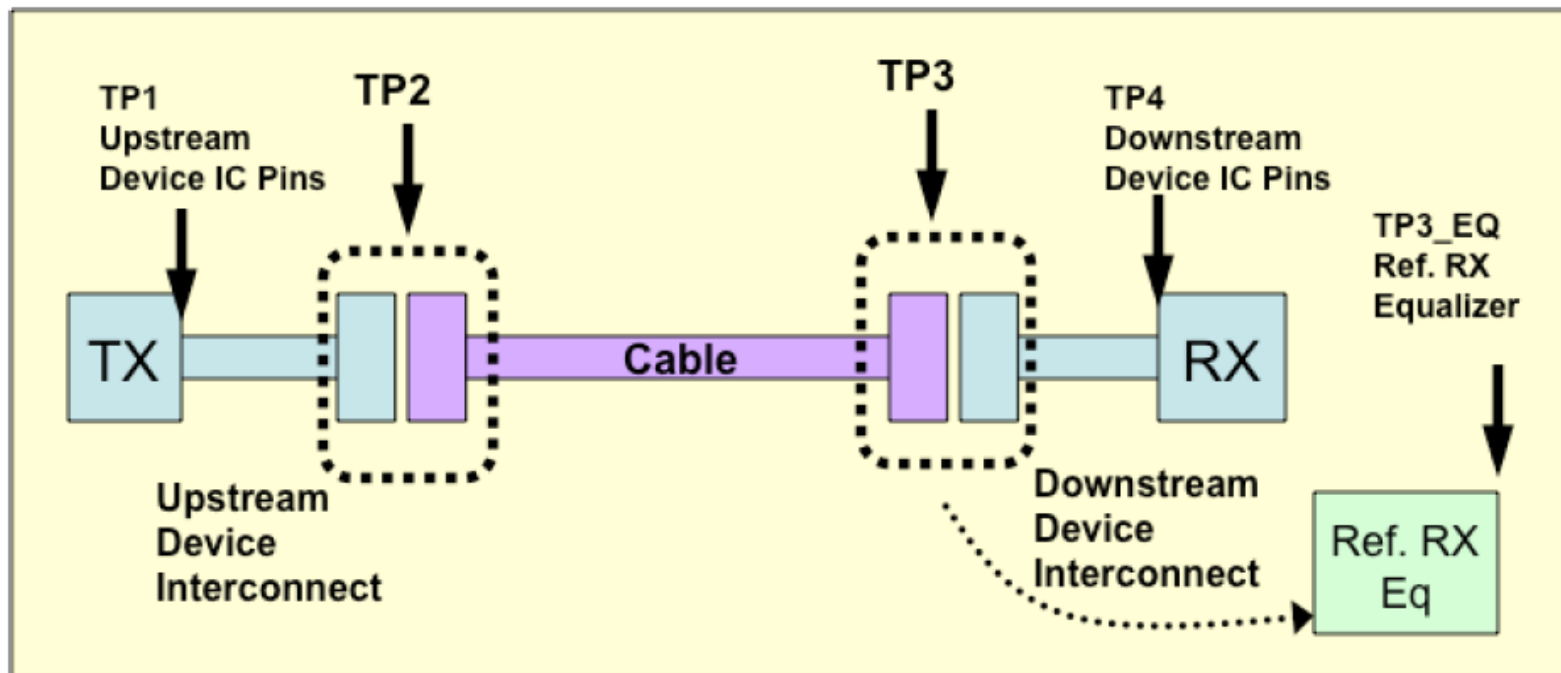
# How does Tektronix help with Display Port testing

- Tektronix offers a complete and easy testing solution to support the testing needs for Display Port.
- Compliance and Characterization.
  - Minimum user intervention
  - Easy Pass fail status
  - Test result provide margins
- Debugging
  - Automatic saving of the failed data set.
  - Offline failure analysis of the save data
  - Flexible probing for debugging

# DisplayPort Test Point

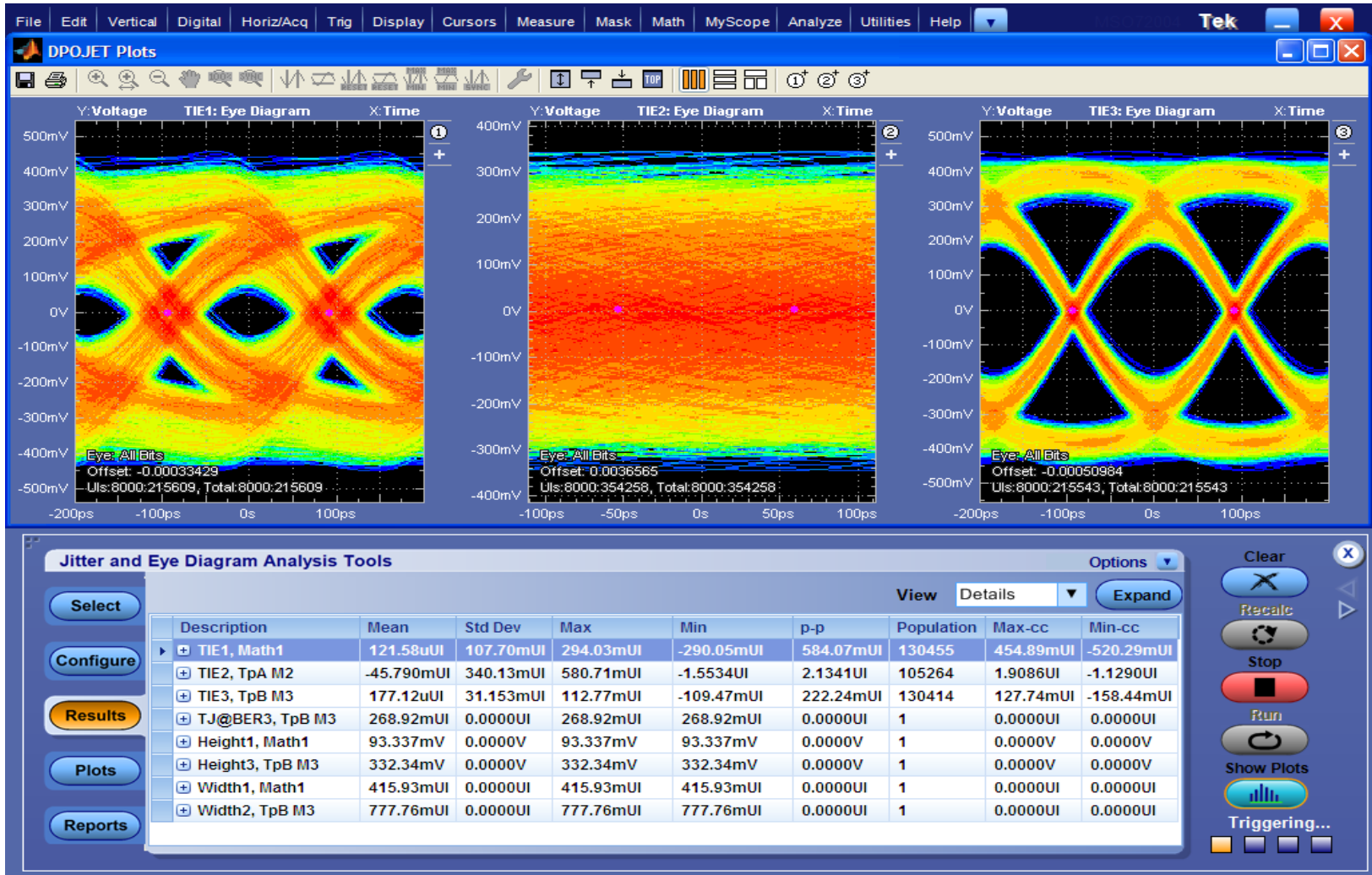
## ■ Test Point Definitions

- TP1: at the pins of the transmitter device.
- TP2: at the test interface on a test access fixture
- TP3: at the test interface on a test access
- TP3\_EQ: TP3 with equalizer applied.
- TP4: at the pins of a receiving device.



# Eye Diagram Test using Eye Compliance Pattern

- An Eye diagram test for 800mV , 0dB pre-emphasis at TP2,TP3, TP3-EQ.



# Automation: DP Testing is a large task!

## Combination Parameters For DP1.2 testing

Data Rate	- 3
Lanes	- 4
Pre-Emphasis	- 4 Levels
Voltage Swing	- 4 Levels
Post Cursor2	- 4 Levels
SSC	- 2 Levels(SSC On and Off)
Patterns	- 5 Supported Patterns

## Combination of tests

1. Differential tests
2. Single Ended tests

Test	Waveforms(SSC, 4 Lanes possible Combinations)
Eye Diagram test	80
Pre-Emphasis Test	240
Non-Pre-Emphasis	32
Total Jitter	80

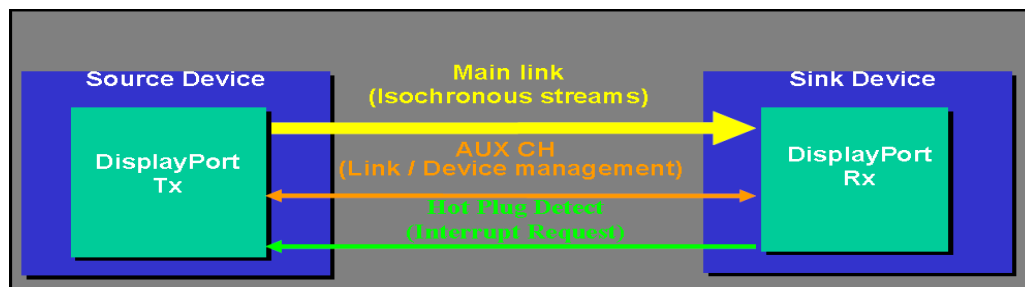
**~432 Acquired signals for DP1.2 Normative Measurements per lane.  
X4 lanes results in 1728 Automated Acquisitions per DUT.**



# DisplayPort Auxiliary Channel Controller (DP-AUX)

## *Why use Aux channel controller in physical layer testing?*

- Speeds up Test Time – No User Interaction is Required to Change Source Output Signal or Validate Sink Silicon State or Error Count
- No Need to Learn Vendor-specific Software - A Single GUI Supports All Vendors
- View & Log Decoded AUX Traffic and Hot Plug Detect (HPD) Events from the Device under Test to the DP-AUX DisplayPort AUX Controller
- Ability to Read and Write DPCD Registers Supports Debug Activities
- Tektronix DP-AUX can serve as a DP1.2 Sink, enabling the source to transmit the required patterns for testing.

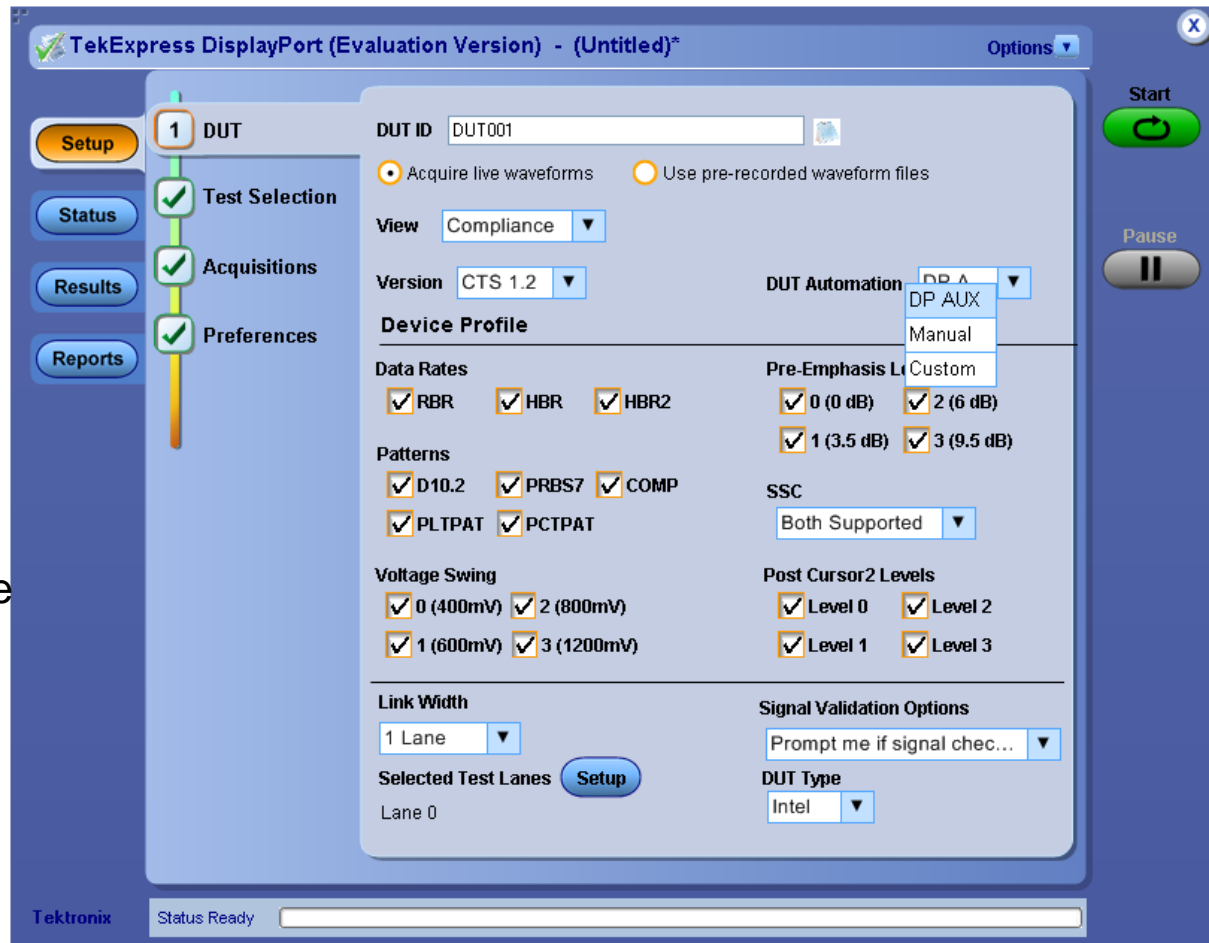


# TekExpress DP1.2 Automation

- Comprehensive Display Port version 1.2 Physical Layer Conformance and Compliance verification tool.

- All Core DP1.2 measurements
- Keithley RF Switch and DP-AUX fully automated solution.
- Selected measurements can be applied across all test permutations (SSC, CTLE's, swing, rates, pre-emphasis, etc) translates to **1728 measurements**. DP12 will provide full user intervention free, automated testing. This is the killer value proposition.

- Factory Automation API for full product control in silicon automation systems.
- Complimentary Fixtures and Compliance Interconnect Channel HW defined by VESA make this package a full customer solution with no compromises.



# DP1.2 Test Selection

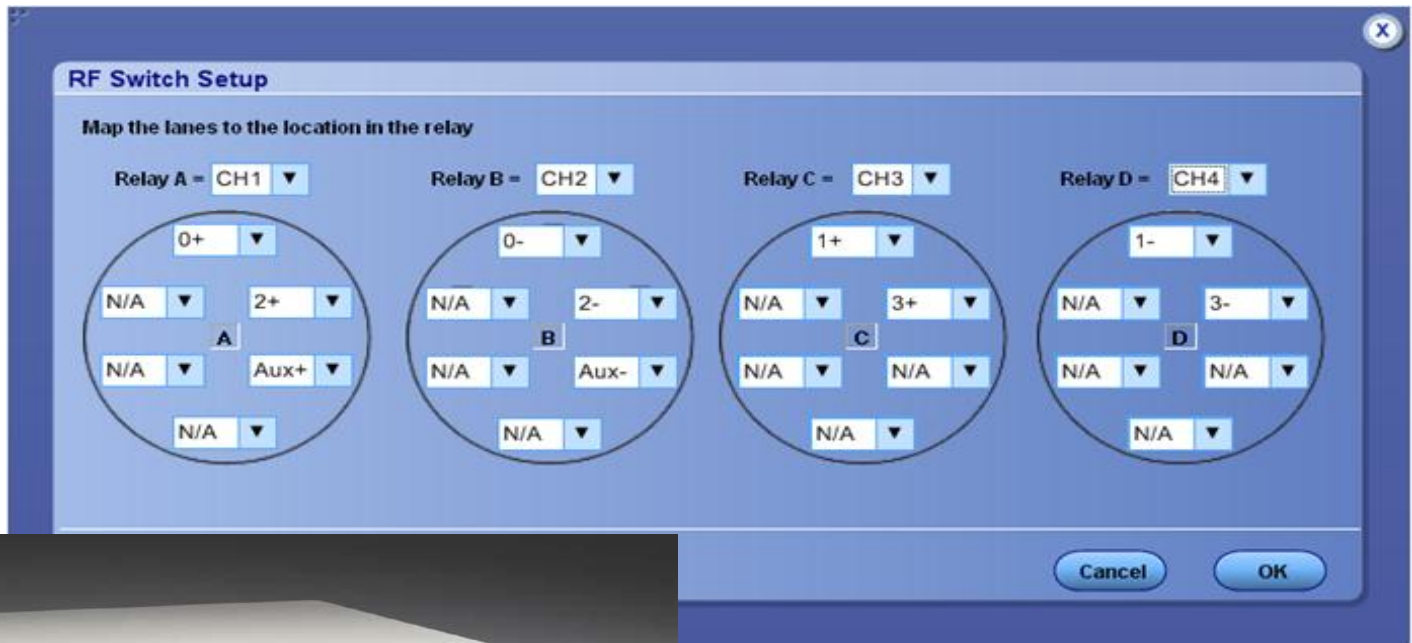
## DP1.2

- Measurement selection is now provided as a function of the user specified test target capabilities.
- If Post Curser 2 capabilities are not present in the DUT, the measurement list will not show them.
- Configuration schematics and online help available for all measurements

The screenshot displays the TekExpress DisplayPort (Evaluation Version) software interface. The title bar reads "TekExpress DisplayPort (Evaluation Version) - (Untitled)\*" with an "Options" dropdown menu. On the left, a vertical navigation pane shows four steps: "Setup" (orange), "2 Test Selection" (blue and highlighted), "Acquisitions" (green), and "Preferences" (green). Below the navigation pane are buttons for "Status", "Results", and "Reports". The main area shows "Device : Source : CTS 1.2" with "Deselect All", "Select Required", and "Select All" buttons. A tree view under "TSG" lists 17 tests, all with checked boxes. Below the list is a "Test Description" section with a text area and "Schematic" and "Configure" buttons. The bottom status bar shows "Tektronix" and "Status Ready". On the right side, there are "Start" (green), "Pause" (grey), and "Stop" (red) buttons.

# Keithley RF Switch Integration and Automation

- DisplayPort transmitter has both Differential tests and Single ended tests and with the integration of RF switch we have complete automated solution without any user intervention for switching between lanes with both single ended and differential tests in sequential automated passes.

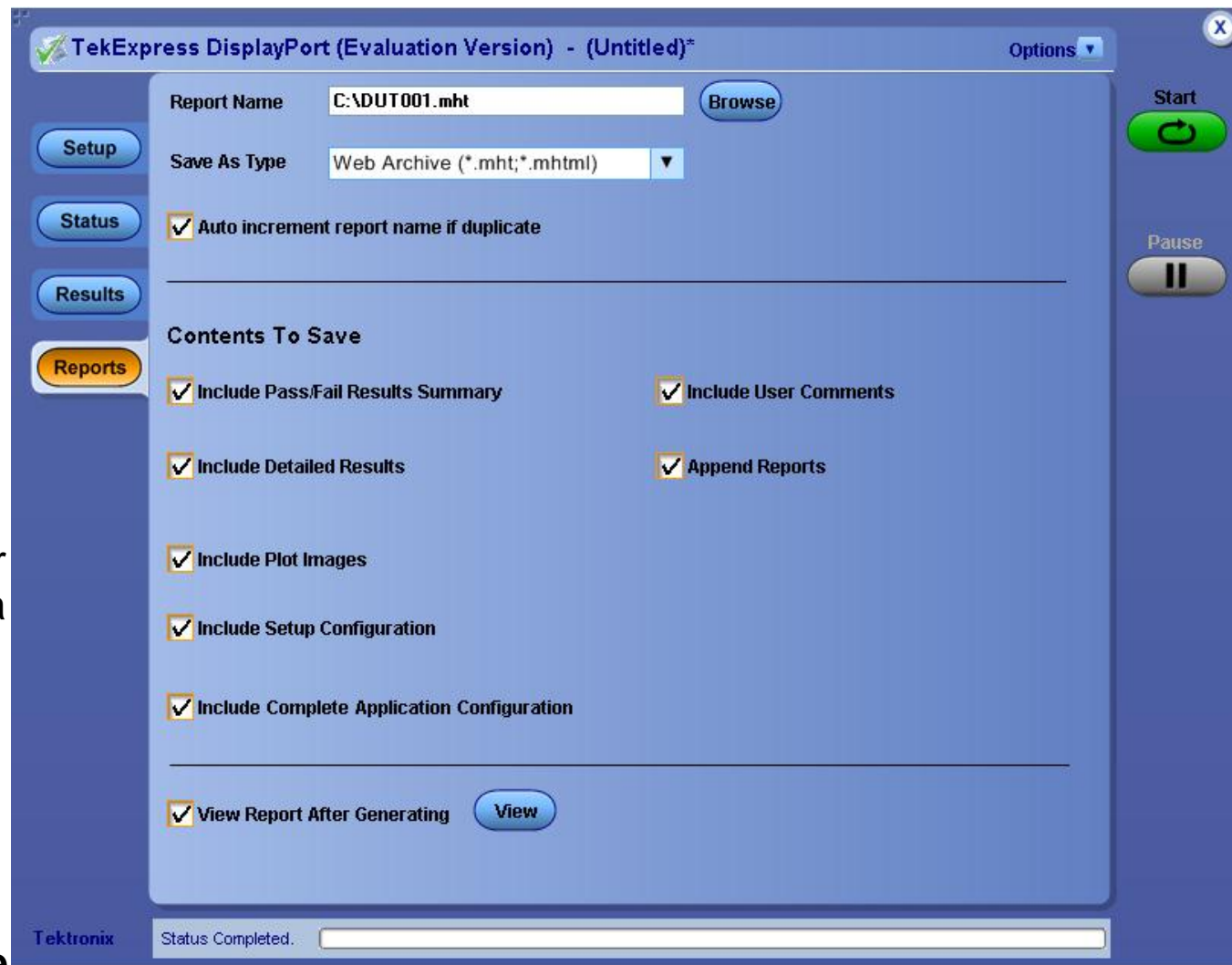


- Keithley is now part of Tektronix.

# DP1.2 Reporting

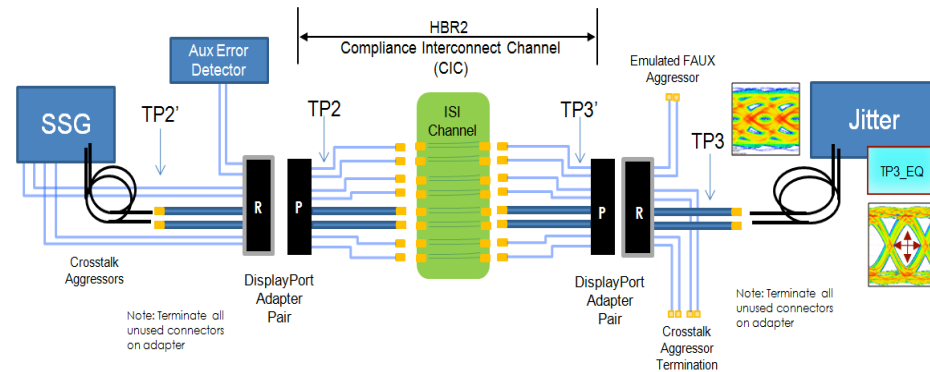
## DP1.2

- Custom html reports which include user specified degrees of detail.
- Reports and Session raw data are stored together allowing recalling a previous run and re-running the test (with different measurement configurations or limits) and re-generating a new report, **without the actual DUT present.**



# Challenges with Sink testing

- Transmitting pattern
  - Three different Complex patterns
- Stressor requirements
  - Rj, Sj, ISI Jitter stressors
  - Cross talk
  - Calibrated with CTLE equalizers
- Error detection
  - Need access to internal register



# Challenges to adding stressors

- Calibration process for all rates
  - Different test points for each type of calibration stress
  - Some stressor are calibrated with any other stressors
  
- What is different between calibrations for the different rates
  - HBR2 contain two SJ tones  
RBR/HBR single SJ tone.
  - HBR2/HBR Tj calibrated at TP3\_EQ,  
RBR Tj calibrated at TP3
  - All three have different duration of testing

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time <sup>1</sup> (seconds)	Data Rate Offset
HBR2 HBR RBR	2 MHz	$10^{12}$	1000	HBR2=185s HBR=370s RBR=620s	0
HBR2 HBR RBR	10 MHz	$10^{11}$	100	HBR2=19s HBR=37s RBR=62s	+350ppm +350ppm +350ppm
HBR2 HBR RBR	20 MHz	$10^{11}$	100	HBR2=19s HBR=37s RBR=62s	0
HBR2 HBR	100 MHz	$10^{11}$	100	HBR2=19s HBR=37s	0

To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR:  $10^{11}$  bits at HBR = 370ps/UI \*  $10^{11}$  UI = 37 seconds)

# What next for Tektronix Display Port tool sets

- Growing segment in Display Port is the Embedded Display Port(eDP)
  - Currently CTS specification is V1.3
  - Specification 1.4 is just release on Sep. 2012, but CTS spec is not ready yet
- Technology is used in Laptops and tables and more
  - eDP used to replace LVDS
  - Sources moving to eDP
  - Display moving at a slower pace
- Solution is a DPOJET plug in using the ADK tool set.
  - Available 4<sup>th</sup> Quarter
  - Support all eDP measurements
  - Printable report



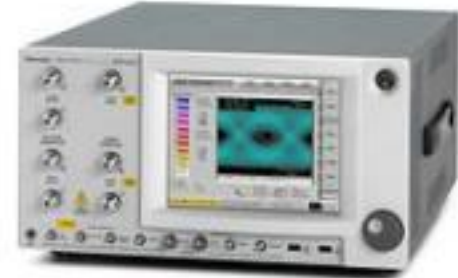
# Complete Tektronix DisplayPort Instrument Portfolio for Source testing

- Equipment for Source testing
  - DSA71254C or higher for HBR2
  - DSA70804C or higher for HBR and RBR
  - P7313SMA for HBR2 (optional)
  - P7380SMA for HBR/RBR (optional)
  - VESA fixtures or Wilder technologies fixtures
  - DP Aux control (Required for Automated testing, optional for manual testing)
  - TekExpress DP12



# Complete Tektronix DisplayPort Instrument Portfolio for Receiver testing

- Equipment for Receiver testing
  - BSA85C
  - BSA12500ISI
  - 100ps TTC qty 2
  - 6 dB attenuators qty 2
  - DC block Qty 2
  - Assorted SMA Cables
  - One to Three way power splitters
  - VESA fixtures or Wilder technologies fixtures
  - DP Aux control (optional if the customer has a way to read the registers)
  - Tektronix Display Port 1.2 MOI





**Tektronix®**