Quicklogic ArcticLink 可编程连接平台解决方案

Quicklogic 公司的 ArcticLink 可编程连接解决方案平台采用 0.18um 六层金属 CMOS 工艺制造,内核电压为 1.8V,I/O 电压可设定为 1.8V,2.5V 和 3.3V. ArcticLink 的逻辑单元为 640 个,集成了高速 USB 2.0 OTG 控制器, SD/SDIO/MMC/CE-ATA 主控制器, ASSP/FPGA 接口,以及灵活的可编程架构,可编程 I/O,非常低功耗模式和安全链接.本文介绍了 ArcticLink 主要特性, 解决方案平台方框图, 连接解决方案方框图,以及各种 USBOTG 连接框图，在汽车内装蓝牙免提，智能手机，PND/PMP 和 ePOS 的应用框图.

The QuickLogic ArcticLink Solution Platform is fabricated on a 0.18 µm, six layer metal CMOS process. The core voltage is 1.8 V. The I/O voltage input tolerance and output drive can be set as 1.8 V, 2.5 V, and 3.3 V.

ArcticLink 器件亮点:

Hi-Speed USB 2.0 OTG Controller

• Single port OTG with embedded high-speed PHY

• Optional 12-signal ULPI interface

• Full-speed CEA-936-A mini-USB analog carkit interface

• Dedicated DMA controller

• High-speed up to 480 Mbits/sec.

SD/SDIO/MMC/CE-ATA Host Controller

• SD/SDIO 1-bit or 4-bit up to 52 MHz with Secure Digital High Capacity (SDHC) support

• CE-ATA 1-bit, 4-bit or 8-bit up to 52 MHz

• MMC 1-bit, 4-bit or 8-bit up to 52 MHz

• High-speed and flexible to support multiple storage options and SDIO peripherals

ASSP/FPGA Interface

• 8 Kbytes scratchpad memory

• Flexible Host interface for USB and SD/SDIO/MMC/CE-ATA ports

• DMA and power management functions

• Direct memory aperture for peripheral subsystems

Flexible Programmable Fabric

• 0.18 µm, six layer metal CMOS process

• 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os

• 36 Kbits of SRAM – seven dual-port 4-Kbit high performance SRAM blocks

• Embedded synchronous/asynchronous FIFO controllers

• One user configurable clock manager (CCM) (110-ball WLCSP and 196-ball TFBGA packages only)

• Up to 120 programmable I/Os available

• 100,000 system gates

• Nonvolatile, instant-on

• IEEE 1149.1 boundary scan testing compliant

Programmable I/O

• Bank programmable drive strength

• Bank programmable slew rate control

• Independent I/O banks capable of supporting multiple I/O standards in one device

• Native support for DDRIOs (196-ball package only)

• Bank programmable I/O standards: LVTTL, LVCMOS, and LVCMOS18

• Can be used for level shifter and I/O voltage translator

Very Low Power (VLP) Mode

• The QuickLogic ArcticLink Solution Platform has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device by placing the device in standby.

• Enter/exit VLP mode from/to normal operation in less than 250 µs (typical)

Security Links

There are several security links to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs.

JTAG

QuickLogic ArcticLink Solution Platform supports IEEE 1149.1 boundary scan or post-manufacturing testability. External access to this feature can be completely disabled.

ArcticLink QL1A100 主要特性列表:

Features		QL1A100
Max Programmable Fabric Gates		100,000
Logic Cells		640
Max I/O		120
RAM Modules		7
FIFO Controllers		7
RAM bits[a]		36,864
CCM (110-ball WLCSP and 196-ball TFBGA packages only)		1
Packages	WLCSP (10 x 11 array)	110
	TFBGA (8 mm x 8 mm)	121
	TFBGA (12 mm x 12 mm)	196
Hi-Speed USB 2.0 OTG Controller with DMA, ULPI Interface and On-Chip PHY		1
SD/SDIO/MMC/CE-ATA Controller		1
Scratchpad SRAM Bytes		8 K

a. There are eight RAM blocks, the last two are concatenated.

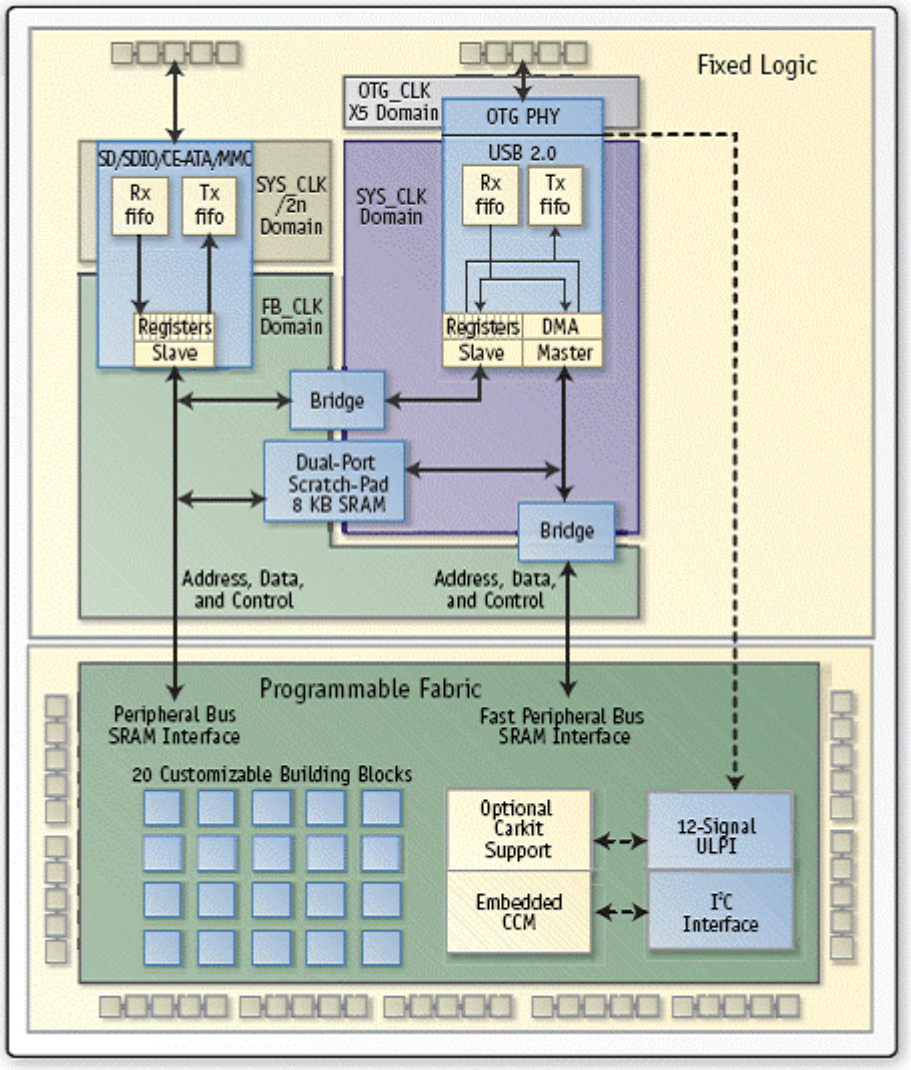

图 1.ArcticLink 解决方案平台方框图

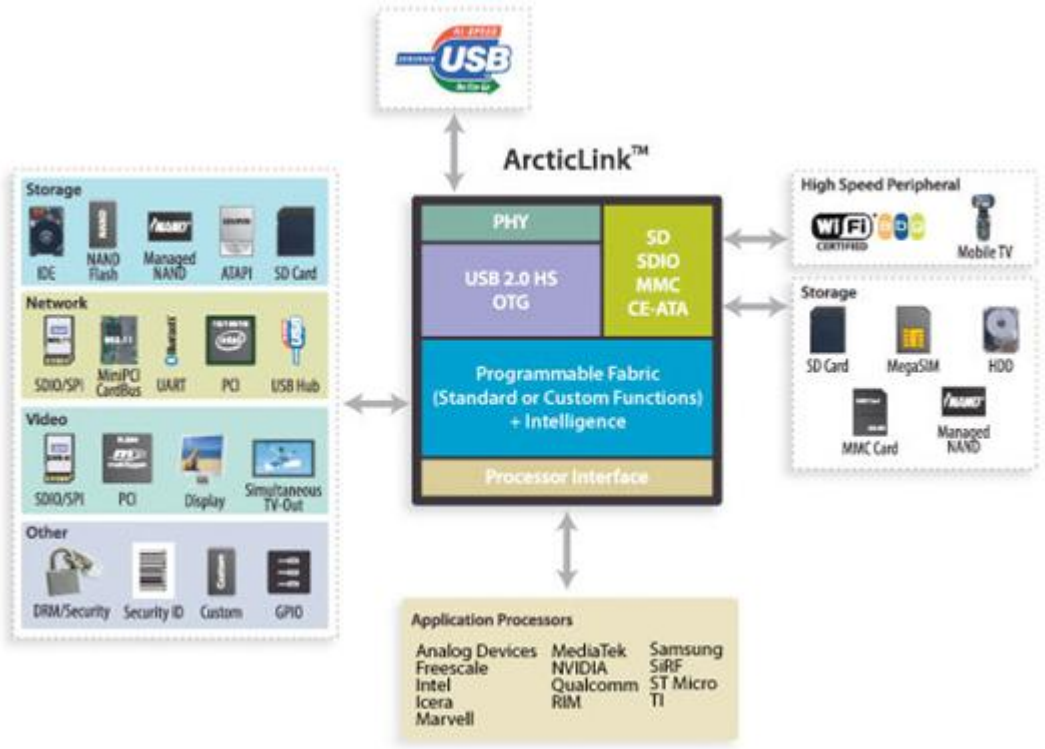

图 2.ArcticLink 连接解决方案方框图

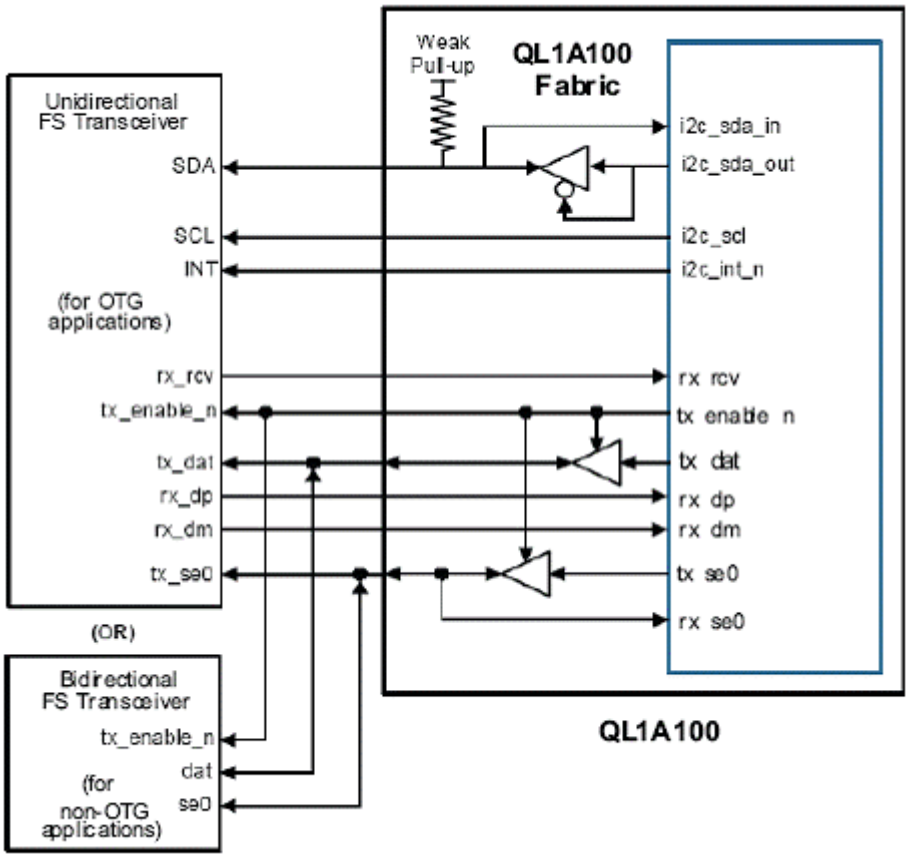

图 3.QL1A100 和 USB 1.1 与 OTG 的连接框图

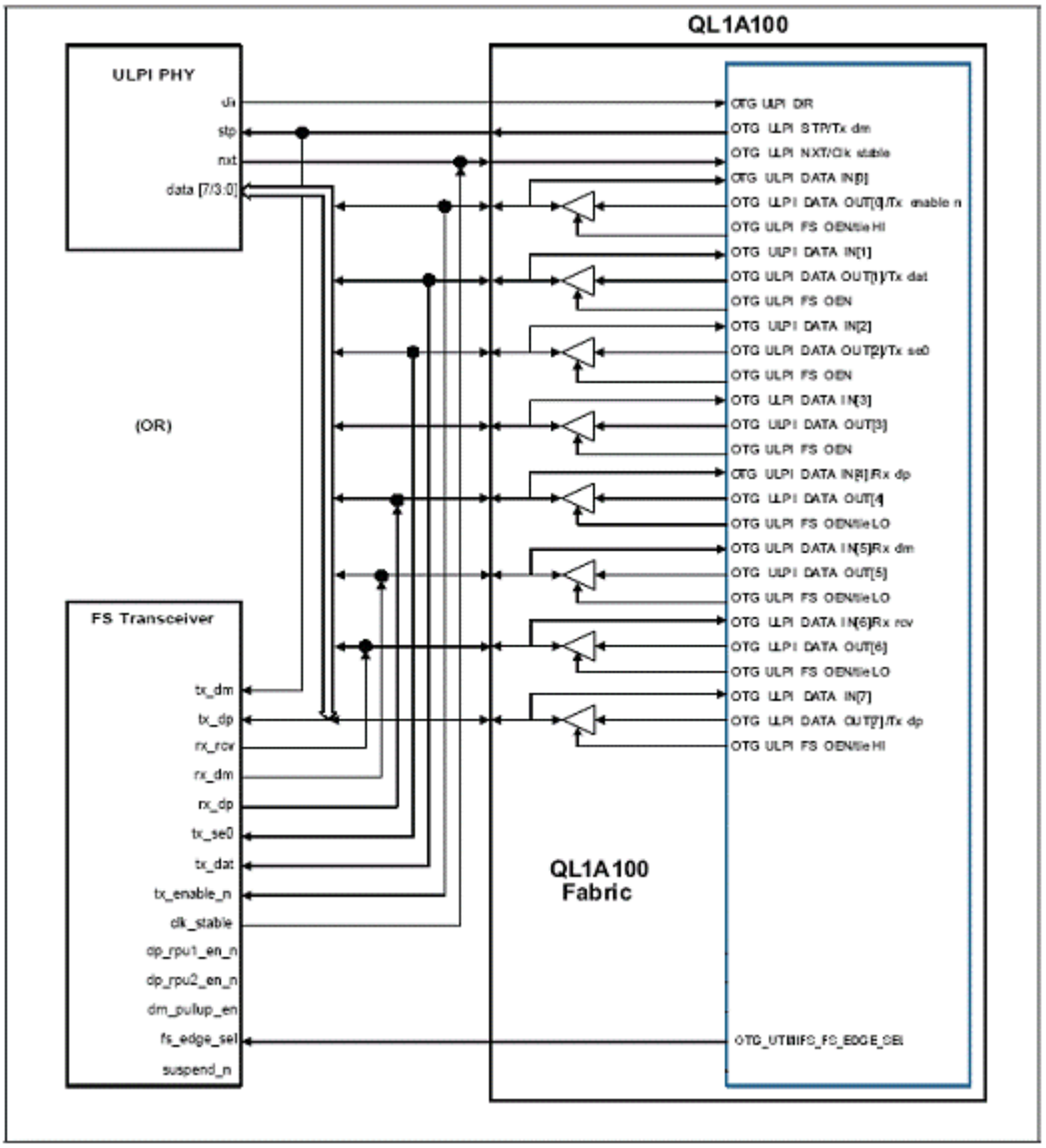

图 4.QL1A100 和 ULPI HS PHY/USB 1.1 串行收发器的连接框图

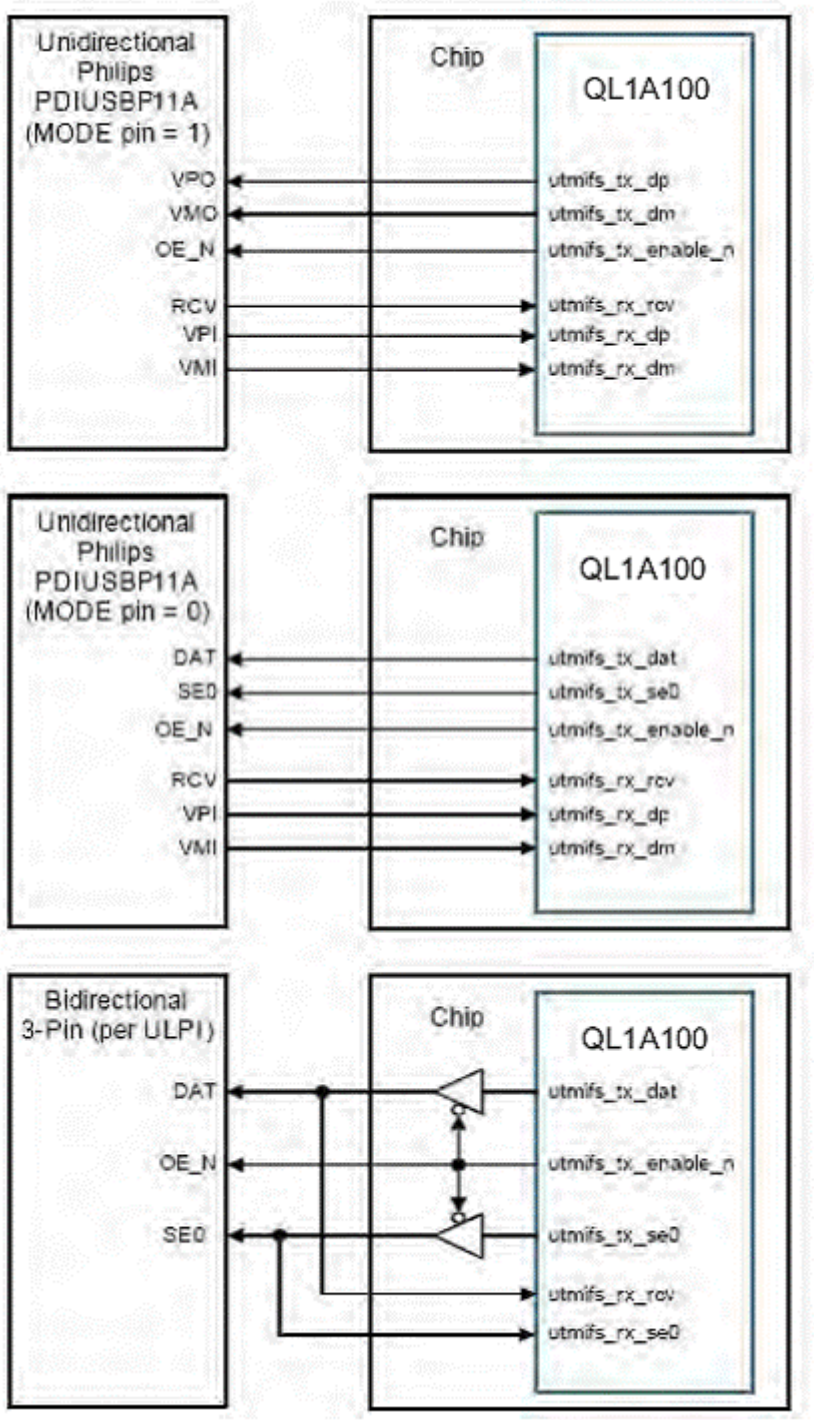

图 5.QL1A100 和 Philips PDIUSBP11A 与 ULPI 3 引脚收发器的连接框图

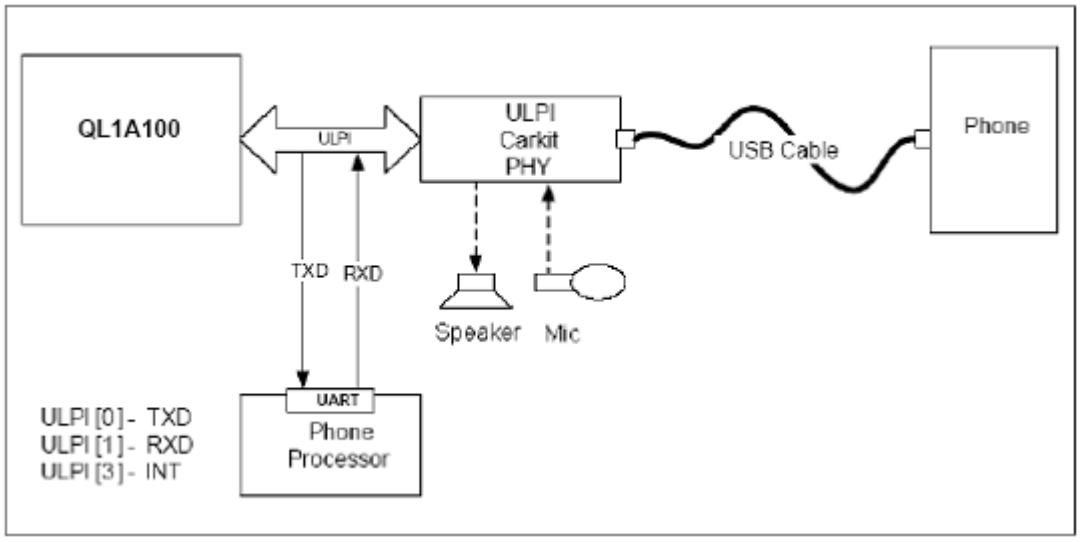

图 6.ArcticLink 在汽车内装蓝牙免提应用框图

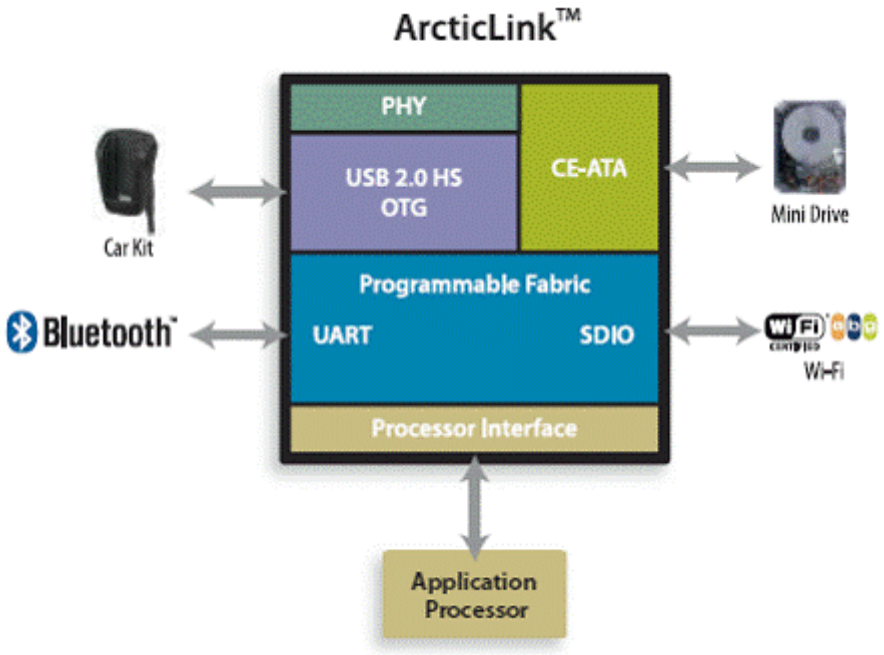

图 7.ArcticLink 在智能手机应用框图

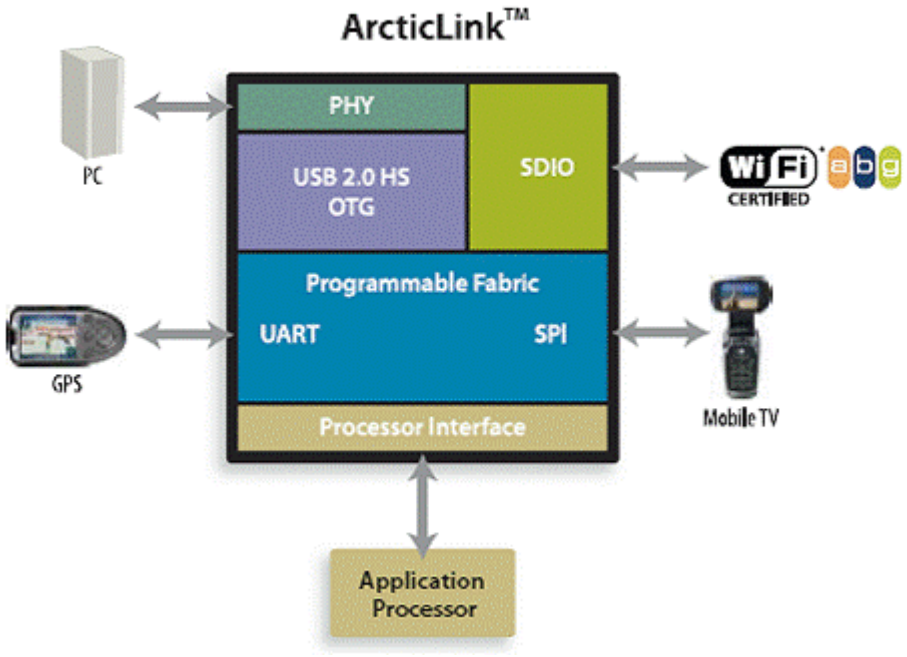

图 8.ArcticLink 在 PND/PMP 应用框图

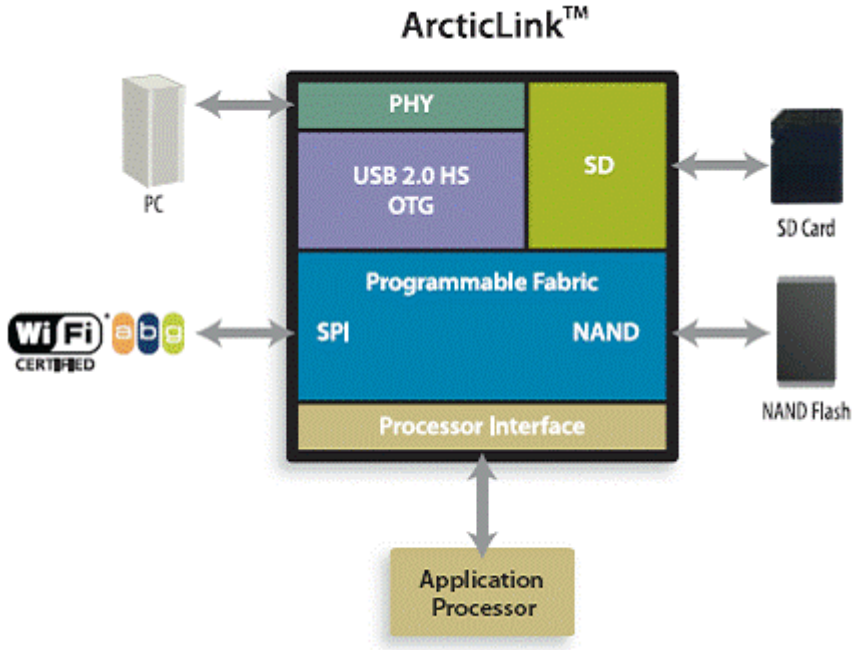

图 9.ArcticLink 在 ePOS 应用框图